

CMOS COLOR/BW DIGITAL VIDEO IMAGE IC

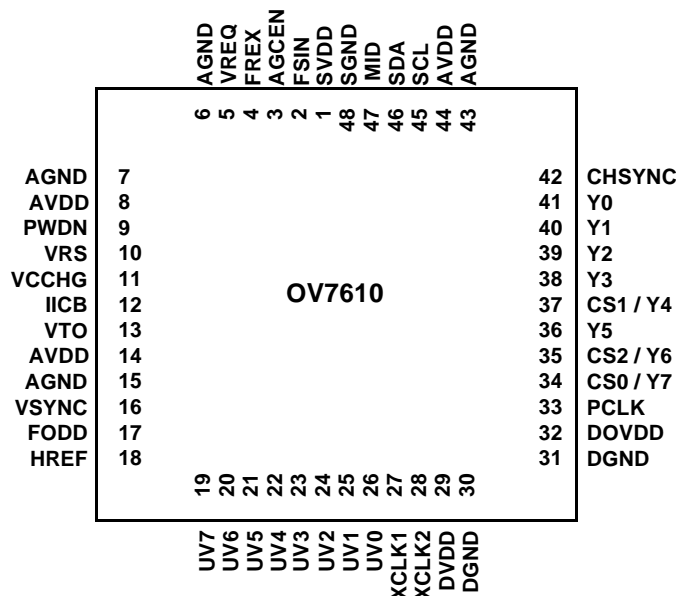
Features

- 307,200 pixels, 1/3" lens, VGA / CIF format
- Read out - progressive / Interlace
- Data format - YCrCb 4:2:2, GRB 4:2:2, RGB Original
- 8/16 bit video data: CCIR601, CCIR656, ZV port
- Video Timing - 525 line, 30 fps
- Wide dynamic range, anti-blooming, zero smearing
- I²C interface
- Electronic exposure / Gain / white balance control
- Image enhancement - brightness, contrast, gamma, saturation, sharpness, window, etc.
- Internal / external synchronization scheme
- Frame exposure / line exposure option
- 5 Volt operation, low power dissipation.

General Description

The OV7610 is a single chip digital color video camera device. It incorporates a 640x480 image array, which is capable of operating up to 60Hz interlace or 30Hz progressive. Based on the proprietary sensor technology, inside the chip, FPN is fully cancelled, smear is eliminated and blooming is drastically reduced. All camera functions, such as exposure, gamma, gain, white balance, color matrix, windowing, are programmable through I2C interface. OV7110 is the uncolored version for monochrome application.

- Video Conferencing
- Video Phone
- Video Mail
- Still Image
- PC Multimedia



Array Elements	644 x 484
Pixel Size	8.4 x 8.4 um
Image Area	5.4 x 4 mm
Electronic Exposure	500 : 1
Scan Mode	progressive interlace
Gamma Correction	0.45/1.0
Minimum Illumination	20 lux @ f1.4 (3000K)
S/N Ratio	42 dB
Power Supply	5VDC, ±5%
Power Requirements	200mW Active 100uW Stby
Package	48 pin LCC

OV7610 48 Pin Out Diagram

1. Pin Assignment**Table 1. Pin Descriptions** (Pin Type and Default Level: I-1: digital input+100k pull up, I-0: digital input+100k pull down, XI/XO: xtal IO, /S: function set during power up. O/I: digital CMOS level output Bias: power supply bias)

Pin #	Name	Class	Function
1	SVDD	Bias	Sensing Power (+5V) pins.
8, 14, 44	AVDD	Bias	Analog Power (+5V) pins.
29	DVDD	Bias	Digital Power (+5V) pins.
32	DOVDD	Bias	Digital I/O Power (+5V / +3.3V) pins.
48	SGND	Bias	Sensing ground connections. Connect to supply common
6, 7, 15, 43	AGND	Bias	Analog ground connections. Connect to supply common
30, 31	DGND	Bias	Digital ground connections. Connect to supply common
2	FSIN	I-0	External Frame Sync input, rising edge active.
3	AGCEN	I-0	AGCEN = 1 enables the Auto Gain Control. AGCEN = 0 disables it. This pin setting is effective when pin IICB = 1.
4	FREX	I-0	Frame exposure control input, effective in progressive scan only. The positive width of FREX defines the exposure time.
5	VrEQ	1.2V	Internal voltage reference. Requires an 0.1uF decoupling capacitor to ground.
9	PWDN	I-0	PWDN = 1 puts chip in power down (sleep) mode.
10	VrS	4.0V	Internal voltage reference.
11	VcCHG	2.5V	Internal voltage reference.
12	IICB	I-0	IICB = 1 selects the power-up method of programming the internal functions. IICB = 0 selects the I ² C internal register programming method. Results of the power-up method can only be changed by a new power-up or reset sequence.
16	VSYNC	O/I	Vertical sync output. This pin is asserted high during several scan lines in the vertical sync period.
17	FODD	O	Odd field flag. Asserted high during the odd field, low during the even field.
18	HREF	O/I	Horizontal window reference output. HREF is high during the active pixel window, otherwise low.
19–26	UV[7:0]	O/I	Digital output UV bus. These pins are used for 16-bit operation for outputting chrominance data.
27, 28	XCLK1, XCLK2	XO, XI	XCLK1 and XCLK2 are the input/output of the on-chip video oscillator. Nominal crystal clock frequency is 27MHz. If an external clock is used, input to XCLK1, leave XCLK2 unconnected.
33	PCLK	O	Pixel clock output. By default, data is updated at the falling edge of PCLK and is stable at its rising edge. PCLK runs at the pixel rate in 16-bit bus operations and twice the pixel rate in 8-bit bus operations.
34–41	Y[7:0]	O/I	Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus.
34	CS0 (shared with Y7)	I-0/S	ID configuration bit for the I ² C slave ID.
35	CS2 (shared with Y6)	I-0/S	ID configuration bit for the I ² C slave ID.
37	CS1 (shared with Y4)	I-0/S	ID configuration bit for the I ² C slave ID.
42	CHSYNC	O	Digital output for either composite sync or horizontal sync signal.
45	SCL	I	I ² C Serial clock input with schmitt trigger.
46	SDA	O/I	I ² C Serial data, output is open-drain, input with schmitt trigger.
47	MID	I-0	Multiple I ² C slave ID enable. MID = 1 I ² C slave ID is configurable through power up setting in CS(2:0) MID = 0 I ² C slave ID is preset to 42H/43H.

2. Functional Description

The OV7610, shown in Figure 1, consists of a 1/3-inch VGA format color imaging array, the analog processing, timing controls, I²C register controls, dual A/Ds, and digital output port. The output data type is selectable between YCrCb and RGB. Its array supports either VGA or CIF image size. The digital output format is supports standards such as CCIR601 16bit, CCIR601 8 bit, ZV Port and CCIR656.

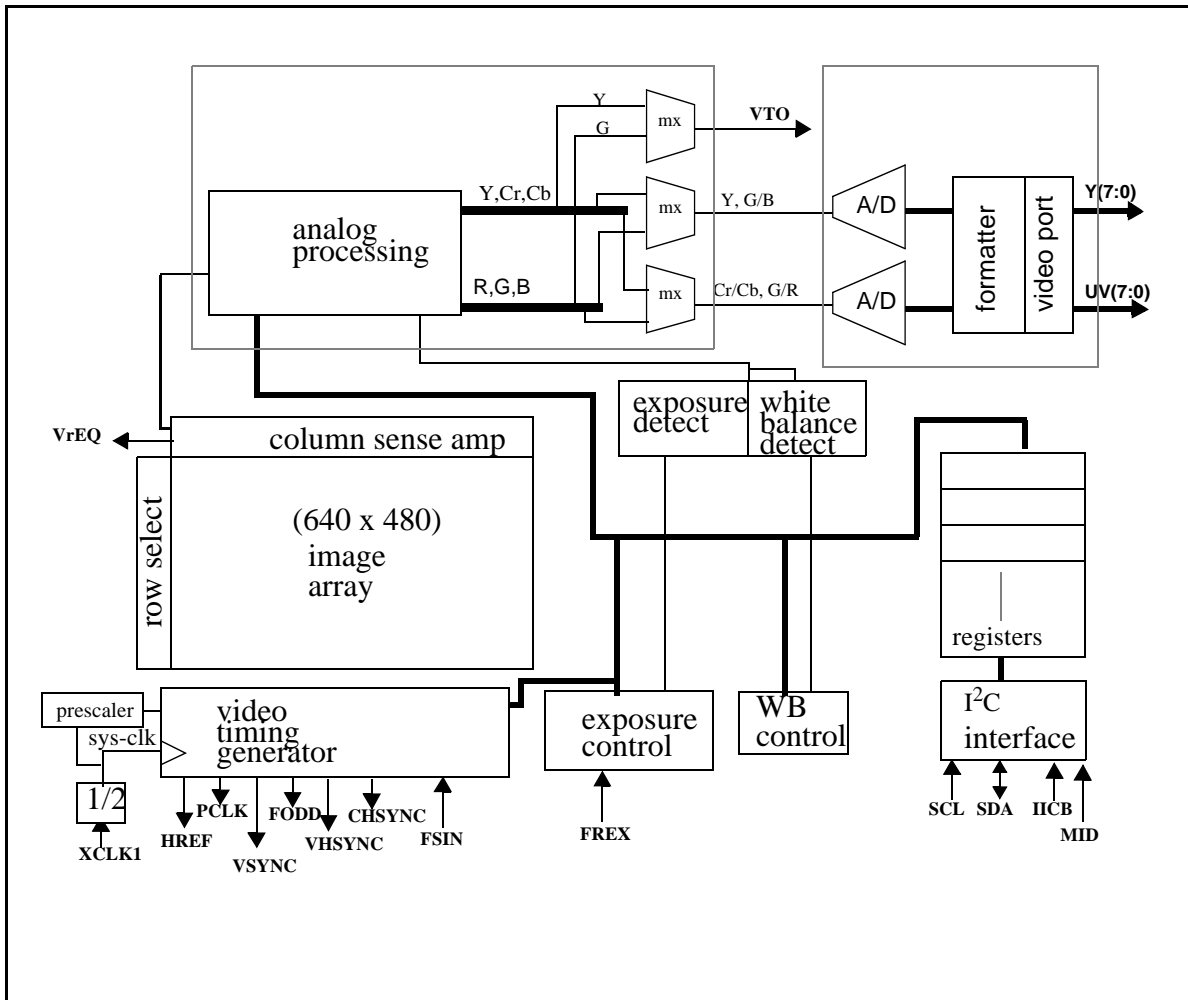


Figure 1. Block Diagram

2.1 Image Data Type

OV7610 supports four image data type: **monochrome**, **raw color pixel**, **YUV422**, and **GBR422**.

The monochrome array is the raw color array before colorations. The raw color array adopts primary Bayer color pattern GR/BG as in Figure 2. Two built-in color space converters map the raw color array to RGB image planes and YUV image planes as shown in Figure 3. Y and G planes are each VGA size, U,V and R,B are each half VGA size. OV7610 can output either original pixel data, the YUV plane or the RGB planes. In either one, the default image size is 640x480 pixels, the maximum image size is 644x484 pixels.

Two ways to obtain the CIF (320x240) image size, one uses the internal subsampling scheme which reduces the full image to 1/4 size, the other uses window function to crop 1/4 portion of the full image.

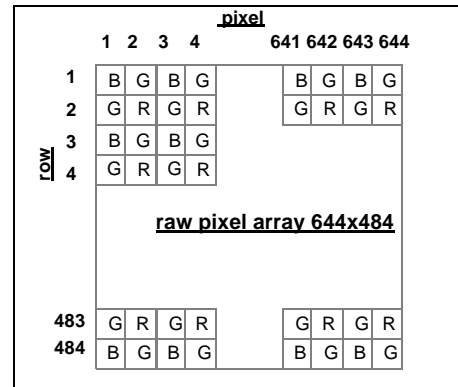


Figure 2. Raw Color Array

2.2 Bus Standards

OV7610 uses two closely tied 8 bit video buses (Y channel and UV channel) to deliver video stream.

In dual channel operation, which includes standards CCIR601-16bit 422, ZV-PORT and straight 16bit data out of A/D, Y channel is either Y image plane data, G image plane data, or Odd line raw pixel data. UV channel is either UV image plane data, RB image plane data, or Even line raw pixel data.

In single channel operation, which includes standards CCIR601-8bit 422, CCIR656 422 and straight 8bit data out of A/D, Y channel is multiplexed data stream taken either from Y/U/V image planes, R/G/B image planes or raw pixel array.

The data format for dual channels is:

- YUV422-
 YYYYY...
 UVUV...
- Raw color array -
 GRGR...
 BGBG...
- GBR422 -
 GGGG...
 BRBR...

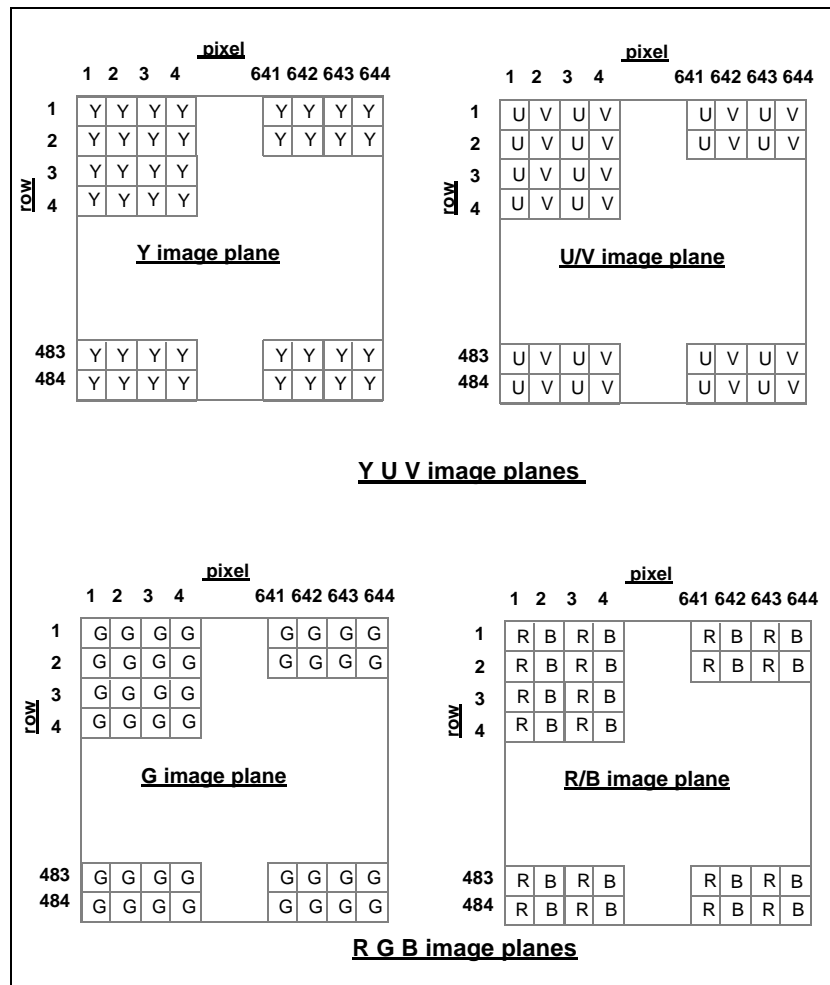


Figure 3. Video Image Mapping (644x484)

2.3 Scan Method

The timing of this device is based on 525 line 60Hz TV standard. There are up to 480 active scan lines in an image. OV7610 can operate in either interlace scan or progressive scan. Interlace scan reads 240 lines in a field, and takes two fields to complete an image frame, progressive scan reads all 480 lines in single field, i.e. each field is an image frame.

Interlace scan, odd line is read in odd field, even line is read in even field, i.e. rows 1,3,5...,479 are read in odd field, rows 2,4,6...480 are read in even field.

Progressive scan, this chip implements various read out schemes to support all image maps.

For Y/UV or RGB image planes, the array is read in row order, i.e rows 1,2,3...480.

For RAW pixel array, the progressive scan has one-line scheme and two-line scheme:

One-line scheme reads one row a time, i.e. rows 1,2,3,...,480.

Two-line scheme reads two lines a time using both Y/UV channels, i.e. the row order for the (Y/UV) channels are: (2/1),(2/3),(4/3),(4/5),(6/5),(6/7)...(478/479),(480/479). * In this case, each row is repeatedly output twice, both contains the same image information.

2.4 Data Order

OV7610 allows data(pixel) to be reordered, coupling with various image data types and single/dual channels output, greatly increase the chip flexibility.

For monochrome application,

BW - to route all pixels to Y channel throughout the entire signal path, the result is much balanced signal level.

For RGB application,

YG -to route all 'G' data to Y channel, all 'RB' data to UV channels. This feature takes the advantage of widely used YUV422 postprocessing scheme and apply to RGB planes to become GBR422.

Other format related features :

XUV - to swap the order of U and V in UV plane, or R and B in RB plane.

XY8 - to swap the order of Y and UV, or G and RB in single channel (8bit) operation.

W720 - to extend the image width to 720 pixels by adding 76 black pixels before the 644 regular pixels.

CIF60 - enable the same CIF image in both even/odd filed interlace scan, effectively doubles frame rate,

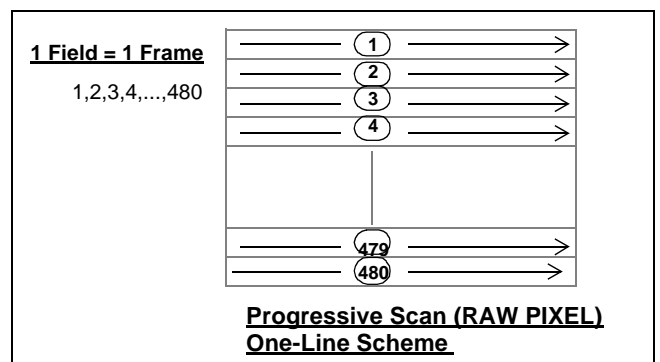
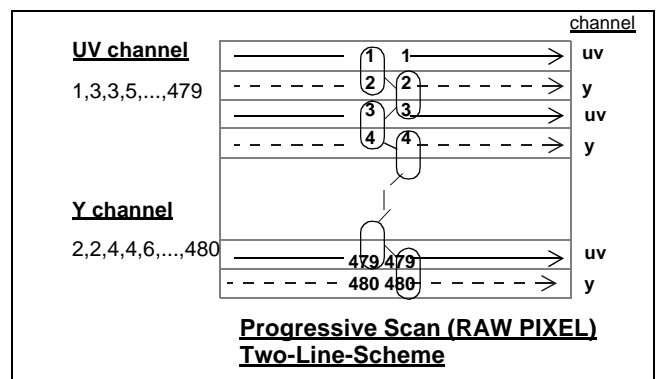
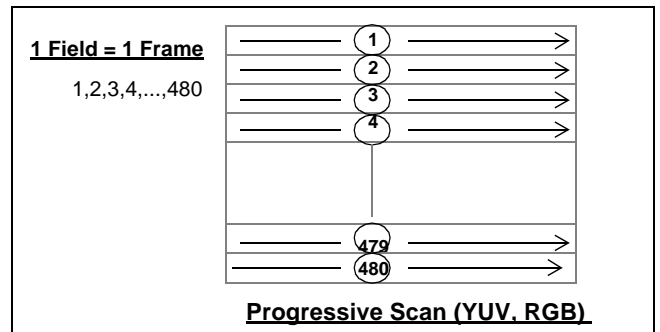
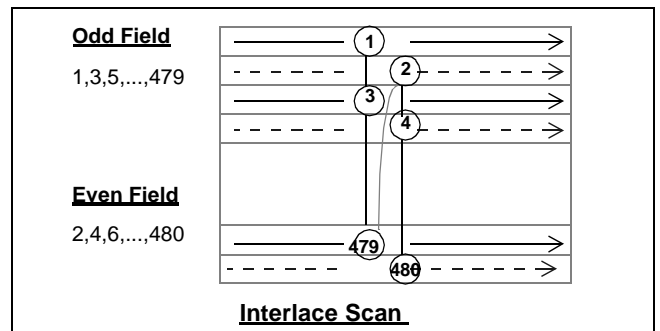


Figure 4. Scanning Schemes

The following table summarize all the available combinations.

Table 2. Data Type & Scan Mode

		Interlace			Progressive		
Resolution		640x480	720x480	320x240	640x480	720x480	320x240
YUV 4:2:2	16Bit	Y	Y	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y	Y	Y
	CCIR656	Y	Y				
RGB 4:2:2	16Bit	Y	Y	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y	Y	Y
	CCIR656	Y	Y				
Y/UV swap ²	16Bit						
	8Bit	Y	Y		Y	Y	
U/V swap	YUV ³	Y	Y		Y	Y	
	RGB	Y	Y		Y	Y	
YG	16Bit	Y	Y	Y	Y	Y	Y
	8Bit						
One Line	16Bit				Y	Y	
	8Bit						

2.5 A/D

The two on-chip 8-bit A/Ds are capable of delivering up to 13.5MS/sec. The operation is fully synchronous to the pixel rate, the actual conversion rate is determined by the clock prescaler. The operation of A/D is completely auto, which requires no user intervention.

2.6 Exposure control

The built-in auto exposure algorithm is optimized for normal scene, where the subject is well-lit compared to the background. Along with the AEC on chip, is the AGC, which can boost to its maximum gain. Since the internal AEC has a range of 500:1 (progressive) and 1:250 (interlace), for most applications, the camera's AEC can adjust itself to match the lighting condition without user intervention. AEC/AGC can be disabled, in this case, manual exposure and gain setting can be done through programming registers "Exp,Gain".

2.7 White balance & Color Temperature Correction

OV7610 maintains color consistency by channel balancing. A well balanced channels ensures image is truly white balanced. The white balance operation can be performed automatically or manually.

Individual registers are available to fine tune the ratio of red and blue components, providing a simple means to correct the color temperature.

2.8 Clock Prescaler

OV7610 includes a clock prescaler. This allows master clock to be divided down to achieve different frame rate other than the standard 60Hz under 27Mhz input clock frequency. One application is to slow down internal clock by in order to increases chip sensitivity. The other application is to adjust frame rate to match with utility power frequency in order to reduce flickering.

2.9 Windowing

The windowing feature allows users to size the window for cropping purpose. The window is sizable from 4 x 4 to 644 x 484 and can be placed anywhere inside the image boundary. Referring to window formula described in the register section.

Note: This function does not change the frame rate or data rate. It simply changes the assertion of the HREF to match the horizontal and vertical region that is programmed by the user.

2.10 Interface Support

OV7610's timing is based on standard 60Hz TV standard. The composite sync timing is available in certain package in pin CHSYNC. Odd field indicator is through pin FODD and vertical sync timing is in pin VSYNC. HREF, PCLK are required for CCIR601 and ZV-port format.

2.11 Multiple Chip Synchronization

Pin FSIN serves as external frame sync input and is positive edge sensitive. In this operation, OV7600 still outputs VSYNC, HSYNC and PCLK, except VSYNC is in sync with FSIN.

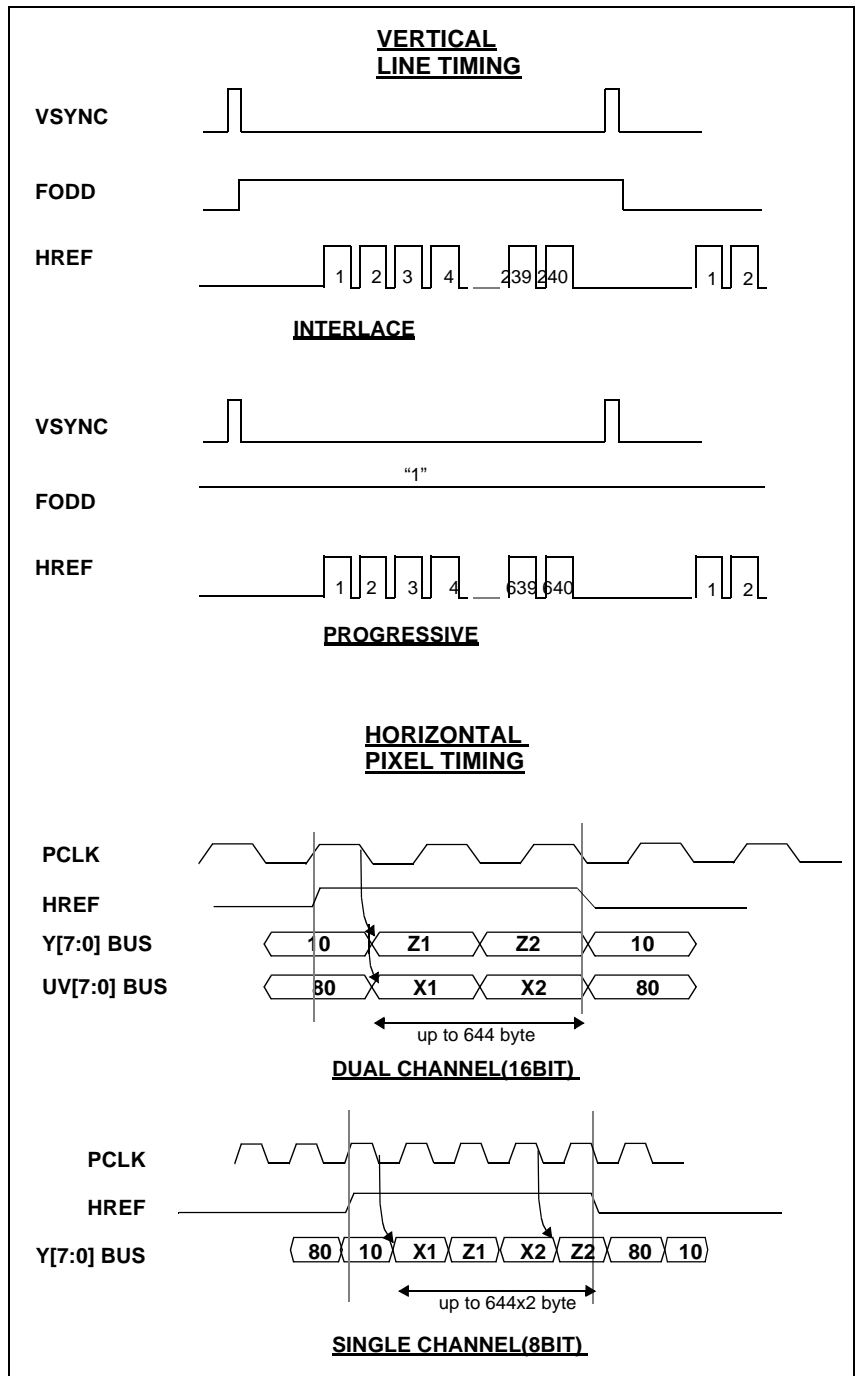


Figure 5. Video Capturing

3. External Sync Operation (Slave mode)

By default, OV7600 operates in master mode, i.e. Hsync,Vsync are outputs signals. However, this device can operate in slave mode, i.e. Hsync, Vsync are inputs. To operate, first switch to slave mode so I/O direction is switched,

External master provides: Clk, Hsync, Vsync;
 Timing requirements: Hsync = 858 CLK, Vsync = 1050 Hsync.
 Chip outputs: PCLK, HREF.

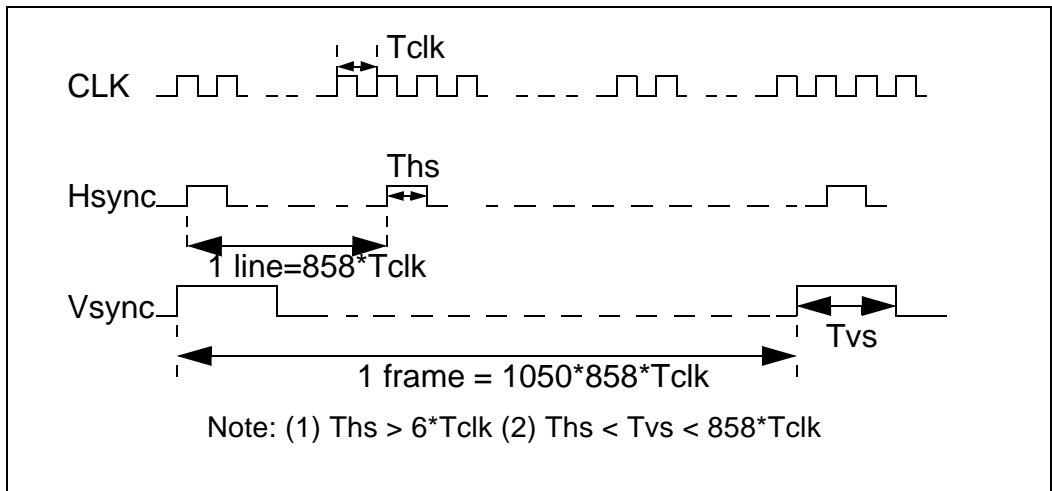


Figure 6. (Slave Mode) External Sync

4. Multiple chip Synchronize

FSIN is an external frame sync input used to sync multiple camera device together. In this application, OV7610 is still operated in master mode, but vertical timing is synchronized to an external **VSINC** input. A simple example is to use one OV7610 as a **VSINC** provider, and the 2nd camera will be sync to it. This **VSINC** is feed to the 2nd OV7610 **FSIN** pin, set the 2nd OV7610 COMC4=1, two cameras are automatically in sync. If using other sync source, to ensure proper operation, the sync trigger pulse must be at least 6 T_{sys} (system clock period, which is decided by CLK<5:0> register) and period will be $1050 * 858 * T_{sys}$.

5. Image State Output

OV7600 provides image information through Y channel, allowing external controller to implement auto exposure auto gain and auto white balance algorithm.

1. Line luminance average level - **Ylav**;
2. Field/frame luminance average level - **Yfav**;
3. Field/frame Green component average level - **Rfav**;
4. Field/frame Red component average level - **Bfav**;
5. Field/frame Blue component average level - **Gfav**.

If enabled, both line and field image information are available:

5.1 Line State

The pixel data is averaged per line and attached to the last 4 bytes of the Y channel video data within each HREF window. In case of YUV planes, the Y data is averaged. In case of RGB planes, G data is averaged. In CIF size, the last 2 bytes contain the image information.

5.2 Field State

The line pixel information is still attached to the last 4 bytes of the HREF window. Four extra entire image averaged data, Yfav/Rfav/Bfav/Gfav, are attached to the last four lines of valid vertical window.

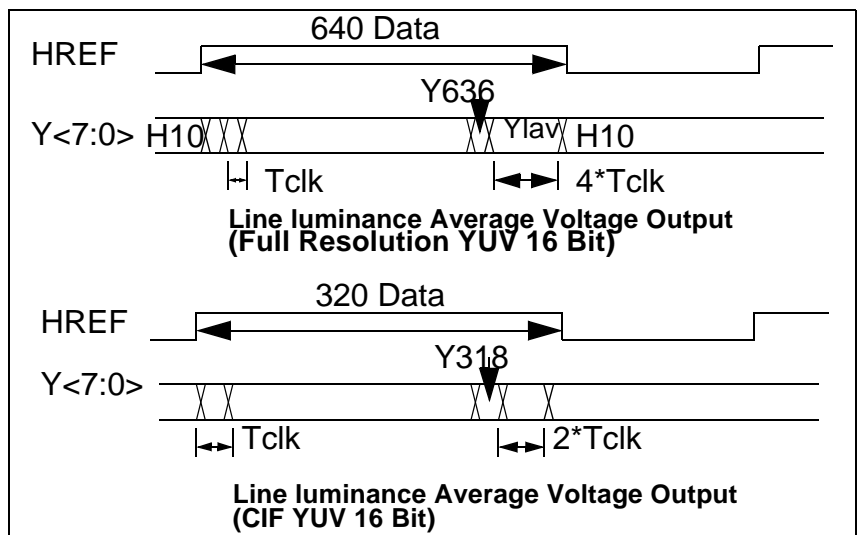


Figure 7. Line State Output

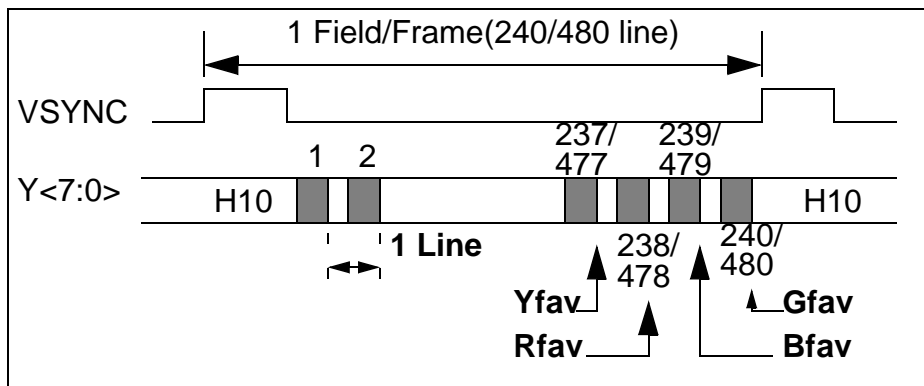


Figure 8. Field State Output

6. Registers & Controls

OV7610 is a full digital imager, all the controls are through I2C registers, it is useful to understand the registers and the internal signal path. Figure 10 & Figure 11 shows detail diagrams for the analog processing and the digital data path blocks. The numbering system in the diagrams indicate the I2C register address and the individual bits associates with each functional element

Analog

6.1 Analog Control

See description

6.2 Digital Control

See description

6.3 System Timing

Internal clock

Register 0x

Register 0x

equal

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Registe

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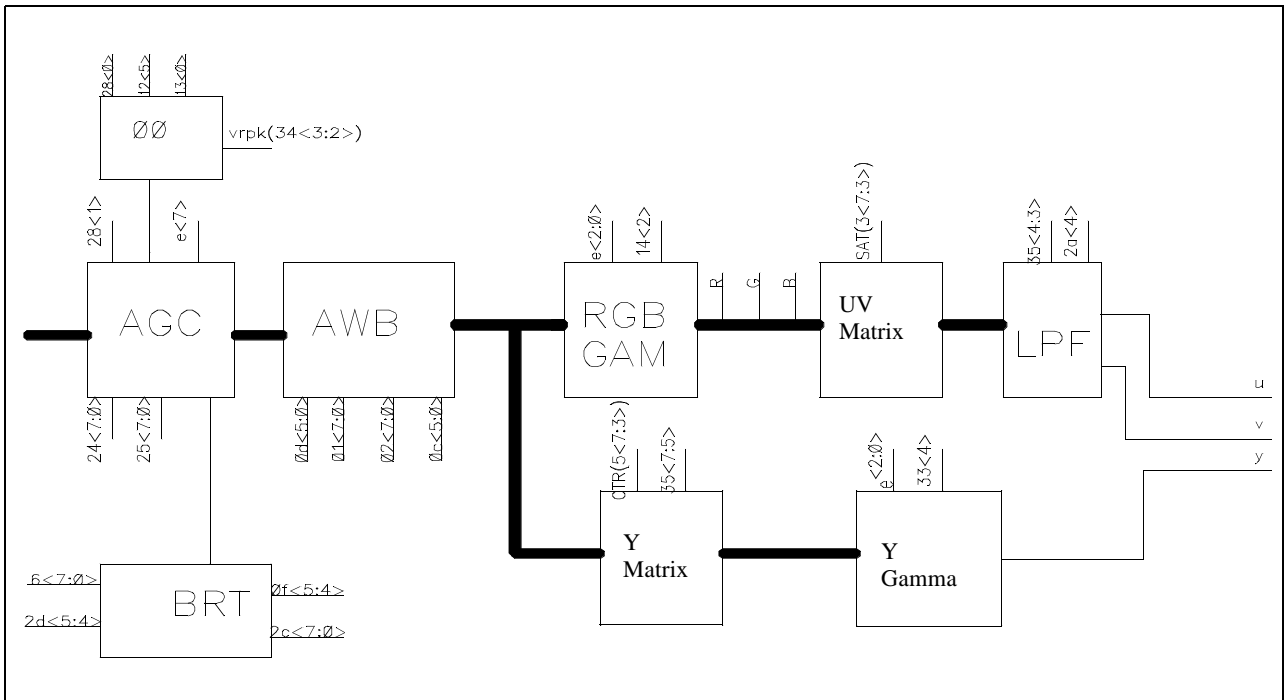


Figure 10. Analog Signal Path Block Diagram

6.4 AGC (Auto Gain Control)

The gain of the circuits is controlled by R00, R28<1:0> & R0E<7>. The formula is

$$\text{Gain} = (R00<3:0>/16 + 1) * (R00<4> + 1) * (R00<5> + 1) * (R28<1> + 1) * (R0E<7> + 1).$$

Setting R13<0> & R12<5> to "0" enables manual gain override.

Setting R13<0> & R12<5> to "1" enables auto gain control.

AGC is a feedback control system, R24<7:0> & R25<7:0> control the loop stability vs response time. A stable system is:

For interlace scan; R24<7:0> + R25<7:0> > 4Dh

For progressive scan; R24<7:0> + R25<7:0> > 9Ah

6.5 AWB (Auto White Balance)

R01, R02, R0C, R0D controls white balance. R01 & R02 adjusts the gross red and blue components to cancel the circuits variations and can be auto or manual, R0C and R0D are manual control to bias the red and blue components for finer color temperature control.

Setting R13<0> & R12<2> to "1" enables auto AWB, no need to adjust R01 & R02.

R0C and R0D : range of control roughly equals rotating UV by ± 30 degree.

6.6 RGB to YUV matrix

YUV matrix is designed to realize the function of RGB to YUV. The formula is

$$Y = (0.6 * G + 0.3 * R + 0.1 * B) * R05$$

$$U = (B - Y) * R03$$

$$V = (R - Y) * R03$$

6.7 Brightness

Setting R2D<4> to "1" enables auto level control, brightness is defined internally.

Setting R2D<4> to "0" enables manual brightness, use R06 to adjust the picture brightness by ± 100mv

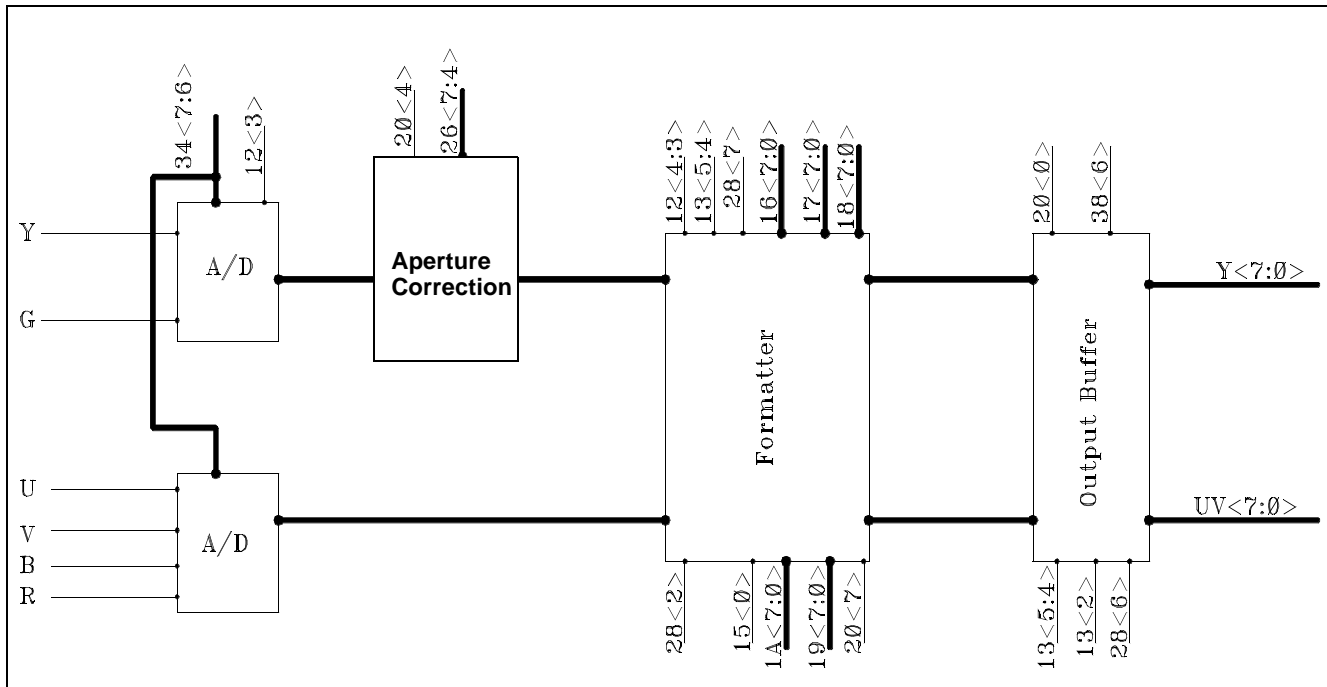


Figure 11. A/D & Digital Data Path Block Diagram

6.8 Dual A/D Converter

Internal dual 10 bit A/D used for YUV and RGB conversion.

Register 0x12<3> select YUV data or RGB raw data output.

Register 0x34<7:6> control A/D reference level and relative output level.

A/D gain equals: [00] is 1, [01] is 0.9, [10] is 0.84, [11] is 0.75

6.9 Digital Aperture Correction

DAC block is luminance edge enhancement block.

Register 0x20<4> is enable/disable edge enhancement.

Register 0x26<7:4> control edge enhance strength. 0x26<7:6> select edge enhance threshold value. Only neighbour pixel luminance signal difference is larger than this threshold, this edge can be enhanced. [00] set threshold is 8 mV, [01] set 16 mV, [10] set 32 mV, [11] set 64 mV. The bigger threshold, the less the edge will be enhanced.

0x26<5:4> control edge enhance strength. If one edge is larger than threshold, then one component will be added to this edge. [00] and [01] select this component will be half of the luminance difference. [10] will be the same difference, [11] will add two times of the luminance difference.

6.10 Formatter

Formatter select different output mode.

Register 0x12<4> select 8 bit output, sequency is YUYV...

Register 0x12<3> select RGB raw data output

Register 0x28<7> select RGB raw data output format is One Line output. Only for Progressive Scan Mode. Only use Y<7:0> output port and every line time only output this line data.

Register 28<2> select RGB raw data output G component from Y<7:0> port and B/R data from UV<7:0> port

Register 0x15<0> control U/V sequency. 0 - VUVU; 1- UVUV

Register 0x20<7> select 720 pixel output mode. Add 80 black pixel before 640 active pixel.

Register 0x16<7:0> control field/frame output selection. Can select all field/frame, even field or odd field output only and drop some of field/frame output.

Register 0x17<7:0> and 0x18<7:0> select output horizontal window size.

Register 0x19<7:0> and 0x1A<7:0> select output vertical window size.

6.11 Output Buffer

Data output buffer block control drive ability.

Register 0x20<0> double output drive current.

Register 0x38<6> double output drive current.

Register 0x13<2> tri-state all data output port.

Register 0x28<6> select B/W mode and only use Y<7:0> port and tri-state UV<7:0> port.

Register 0x13<5:4> only enable Y<7:0> port and tri-state UV<7:0> port.

7. I²C Bus

Pin IICB = 0 selects the I²C access. The OV7610 is an I²C slave device that supports 400 kbps, 7-bit address data transfer protocol as shown in Figure 12. on page 14.

“Restart” feature is not supported here. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Standard I²C requires only two pins: SCL and SDA. SDA is configured as open drain for bidirectional purpose. A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions. Except these two special conditions, the protocol requires SDA to be stable during the HIGH period of the clock SCL. Each bit can only change state when is SCL LOW. See Figure 13. on page 15.

7.1 I²C Bus Protocol

The I²C access is enabled only if pin IICB = 0. The OV7610 is a slave device that supports 400 kbps, 7-bit address data transfer protocol.

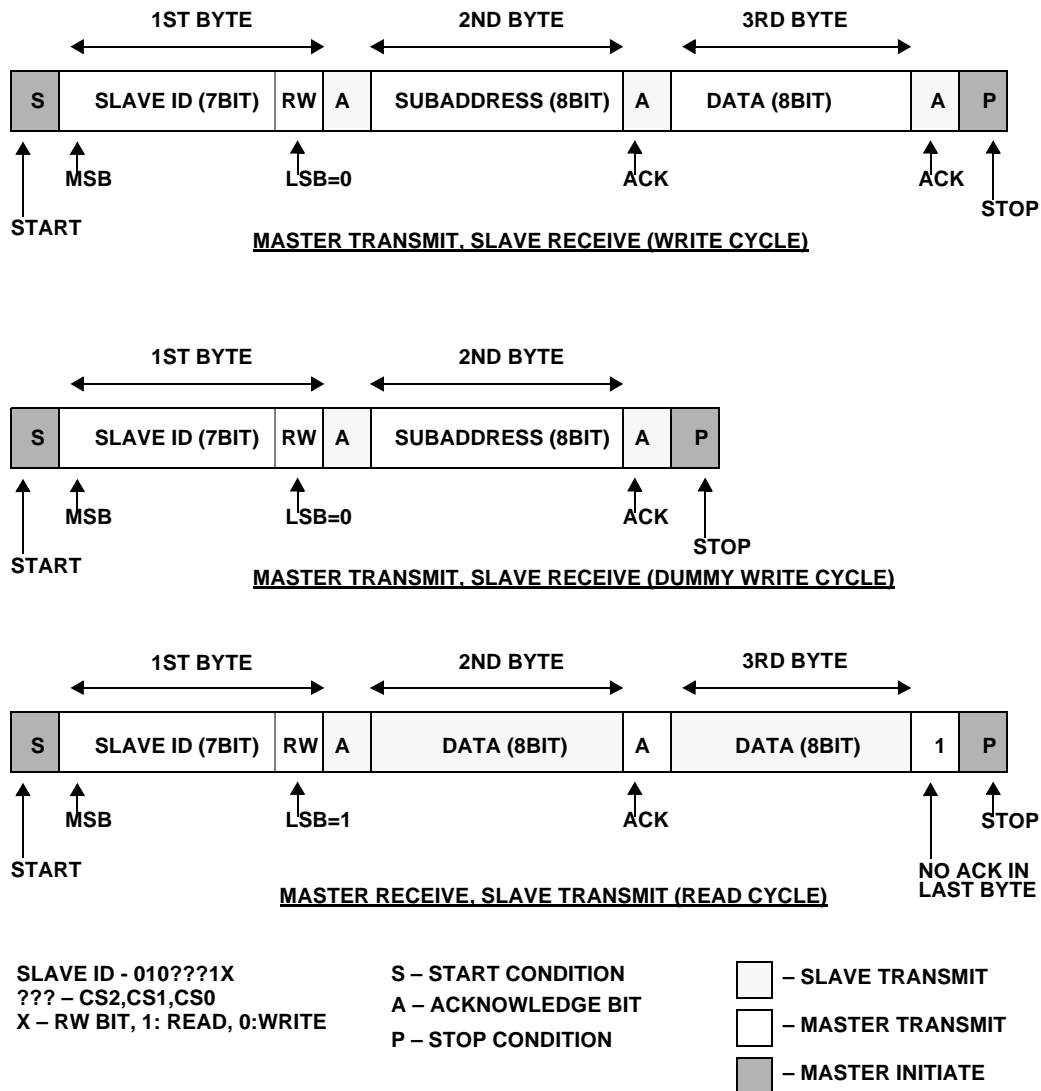


Figure 12. I²C Bus Protocol Format

Note that the restart feature is not supported here. Within each byte, MSB is always transferred first. Read/write

control bit is the LSB of the first byte. Standard I²C requires only two pins: SCL and SDA. SDA is configured as open drain for bidirectional purpose.

A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions. Except these two special conditions, the protocol requires SDA to be stable during the HIGH period of the clock SCL. Each bit can only change state when is SCL LOW. See Figure 13. on page 15.

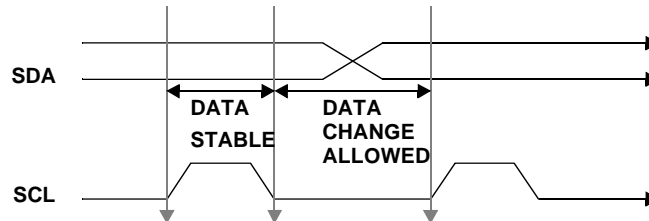


Figure 13. Bit Transfer on the I²C Bus

OV7610 reserves CS[2:0] for the slave ID configuration, which makes eight combinations. In I²C operation, the master must do the following operations:

- **Generate the start/stop condition**
- **Provide the serial clock on SCL**
- **Place the 7-bit slave address, the RW bit, and the 8-bit subaddress on SDA**

The receiver must pull down SDA during the acknowledge bit time. During the write cycle, the OV7610 returns the acknowledgment and during read cycle, the master returns the acknowledgment except when the read data is the last byte. If so, the master does not acknowledge the last data byte, so that the read cycle can be terminated.

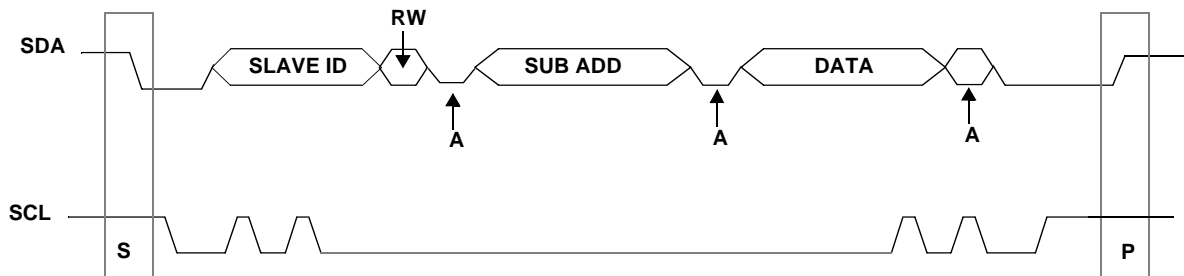


Figure 14. Data Transfer on the I²C Bus

The OV7610 I²C supports multi-byte write and multi-byte read. The master must supply the subaddress. in the write cycle, but not in the read cycle. Therefore, the OV7610 takes the read subaddress from the previous write cycle. In multi-byte write or multi-byte read cycles, the subaddress is automatically increment after the first data byte so that continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original subaddress; therefore, if a read cycle immediately follows a multi-byte cycle, you must insert a single byte write cycle that provides a new subaddress.

The OV7610 supports single slave ID (pin MID=0) and multiple slave ID (pin MID=1). In single, ID is preset to 42/43. In multiple, ID is configured by setting pin CS[2:0] (high or low) to one of the eight combinations listed below at reset or power up.

Multiple Slave ID

CS[2:0]	000	001	010	011	100	101	110	111
WRITE ID(hex)	42	46	4A	4E	52	56	5A	5E
READ ID (hex)	43	47	4B	4F	53	57	5B	5F

In the write cycle, the second byte in I²C bus is the subaddress for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to unimplemented subaddress is ignored. In the read cycle, the second byte is the data associated with the previous stored subaddress. Reading of unimplemented subaddress returns unknown.

7.2 Register Set

Table 3. I2C Registers

Subad- dress (hex)	Register	Default (hex)	Read/ Write	Descriptions
00	Gain[5:0]	00	RW	GC[5:0] – Gain setting. gain=(GC[5]+1)*(GC[4]+1)(GC<:3:0> /16 +1) GC[7:6] - unimplemented bit, returns 'X' when read.
01	Blue[7:0]	80	RW	BLU[7:0] – blue channel balance value. "FFh"- highest, "00h"-lowest
02	Red[7:0]	80	RW	RED[7:0] – red channel balance value. "FFh"- highest, "00h"-lowest
03	Sat	80	RW	SAT[7:0] – saturation adjustment. "FFh"- highest, "00h"-lowest
04	Rsvd04	80	RW	reserved
05	Cnt	00	RW	CTR[7:0] – Y signal contrast adjustment. "FFh"-highest, "00h"-lowest
06	Brt	80	RW	BRT[7:0] – Y signal brightness adjustment. "FFh"-highest, "00h"-lowest
07	Shp	80	RW	SHP[7:0] – sharpness adjustment, "00h"- highest, "FFh"- lowest. * for this to be effective, set COME[5] =1
08 - 0B	Rsvd08 – 0B	-	-	reserved
0C	Blue Bias	20	RW	BBS[5:0] – blue channel bias value. "3Fh"-highest, "00h"-lowest
0D	Red Bias	20	RW	RBS[5:0] – red channel bias value. "3Fh"-highest, "00h"-lowest
0E	Gamma Coeff	8C	RW	GAM[7] - additional 2x gain enable GAM[6] - disable color filter compensation, in BW application, set this bit to "1" GAM[4:3] - S-AWB control 00 - 0.2 01 - 0.4 10 - 0.6 11 - 0.8 GAM[2] – "1" selects value 0.45, "0" selects value 0.5, effective when COMC[2]=1 GAM[1:0] – gamma curve fine tune. 00 - 95% 01 - 90% 10 - 85% 11 - 80%

Subaddress (hex)	Register	Default (hex)	Read/Write	Descriptions
0F	WB Range	05	RW	<p>RWB[7] - AEC method 1 RWB[6] - AEC method 2 RWB[5:4] - ALC black level 00 - 1.20v 01 - 1.24v 10 - 1.26v 11 - 1.28v RWB[3:2] - S-AWB upper level limit 00 - 70% 01 - 80% 10 - 90% 11 - 100% RWB[0:1] - S-AWB lower level limit 00 - 10% 01 - 20% 10 - 30% 11 - 40%</p>
10	Exp	7F(I)/FF(P)	RW	<p>EC[7:0] – Manual exposure setting. <u>Valid range: interlace 00h~7Fh; progressive 00-FFh</u> formula for exposure time: $T_{EXPOSURE} = T_{LINE} \times EC[7:0] \times 2$; where $T_{LINE} = \text{Frame Time}/525$. The actual time of a scan line is determined by the clock rate divider. This register is only effective when operated in manual adjust mode (COMB[0] = 0). Nevertheless, this register is always accessible through the I²C bus. It generally takes no more than two fields for the image to reach the intended exposure after changing the setting.</p> <p>** This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting.</p>
11	Clock	00	RW	<p>CLK[5:0] - system clock prescaler; formula for pixel clock rate: clock rate = (CLK_input / ((CLK<5:0> + 1) / 2)) SYN[7:6] - polarity for sync timing outputs 00: HSYNC, CHSYNC, VSYNC = “- - +” 01: HSYNC, CHSYNC, VSYNC = “- - -” 10: HSYNC, CHSYNC, VSYNC = “+ - +” 11: HSYNC, CHSYNC, VSYNC = “- + +” The effect of the change is immediate, however, it generally takes about two fields for the image to reach the stable state.</p>
12	Common A	24	RW	<p>COMA[7] - “1” initiates the chip soft reset, the reset takes place after the acknowledge bit is issued, the effect is the same as powerup the chip, the chip is initialized to a default state, all registers including I²C’s contents are set to default, this bit is self cleared after the reset. COMA[6] - “1” selects mirror image. COMA[5] - “1” enables AGC, for it to take effect, COMB0 must be set. COMA[4] - “1” swaps Y/UV data in 8 Bit operation, data order YUYV... COMA[3] - “1” selects RGB image plane, “0” selects YCrCb image plane COMA[2] - “1” enables auto channel balance, for it to take effect, COMB[0] must be set. COMA[1] - “1” Color Bar Test pattern. COMA[0] - “1” select Line BLC, “0” enables field BLC.</p>
13	Common B	01	RW	<p>COMB[7:6] - rsvd. COMB[5] - “1” enable 8 bit operation, Y bus is active, UV bus is tri-stated. COMB[4] - “1” enables CCIR656 bus operation, Y bus is active, UV bus is tri-stated. COMB[3] - selects a timing signal to pin CHSYNC; “1” is composite sync, “0” is horizontal sync. COMB[2] - “1” puts Y and UV buses in tri-state. COMB[1] - “1” initiates the single frame transfer, for this function to work, field drop mode (FD<1:0> in REG 16) must set to “OFF”. See Figure 15. on page 21, after this bit is set, HREF is only asserted for consecutive two fields beginning at Odd field. This bit is cleared automatically at the end of this frame. Clearing this bit in the middle of active frame has no effect to the assertion of the current HREF. COMB[0] - main auto adjust mode enable. Once enabled, Reg(00,01,02,10) are set by internal auto control, read of them returns auto set value, write is ineffective because internal control will overwrite itl.</p>
14	Common C	00	RW	<p>COMC[7:6] - rsvd COMC[5] - “1” selects CIF (320x240) image, the image is subsampled from the full VGA frame. COMC[4] - selecting timing signal to output pin VSYNC “1” - frame sync, vertical sync is asserted in every odd field, “0” - field sync, vertical sync is asserted in every field. COMC[3] - Inverting HREF polarity COMC[2] - “1” gamma value set by GAM[2]; “0” gamma value is 1.0. COMC[1:0] - rsvd</p>

Subaddress (hex)	Register	Default (hex)	Read/Write	Descriptions
15	Common D	00	RW	<p>COMD[7] - rsvd COMD[6] - inverting PCLK polarity, "1" - video data change on rising edge "0" - video data change on falling edge, this is the default setting. COMD[5:1] - rsvd COMD[0] - exchanges U V order; "1" - V U V U... 16Bit operation, V Y U Y... 8 Bit operation; "0" - U V U V... 16Bit operation, U Y V Y... 8 Bit operation.</p>
16	Field Divide	03	RW	<p>FD[7:2] – Field interval selection. See Figure 16. on page 22. The feature, together with FD[1:0], divides the video signal into a programmed number of time slots in units of field, and HREF is active only in one field during the period. This function does not affect the video data or pixel rate. Only one bit can be set and the valid combinations and functions are as follows: "000001" – Divide to 2 slots. HREF is asserted every 2 fields. "000010" – Divide to 4 slots. HREF is asserted every 4 fields. "000100" – Divide to 8 slots. HREF is asserted every 8 fields. "001000" – Divide to 16 slots. HREF is asserted every 16 fields. "010000" – Divide to 32 slots. HREF is asserted every 32 fields. "100000" – Divide to 64 slots. HREF is asserted every 64 fields. FD[1:0]- field mode selection. Interlace scan: "00" - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) "01" - ODD mode; HREF is asserted in odd field only. "10" - EVEN mode; HREF is asserted in even field only. "11" - FRAME mode; HREF is asserted in both odd field and even field. Progressive scan: "00" - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) "01,10" - SLOT mode; HREF is asserted in frame according FD<7:2>. "11" - FRAME mode; HREF is asserted in every frame. FD<7:2> useless</p>
17	Horizontal Window Start	38	RW	<p>HS[7:0] - selects the starting point of HREF window, each LSB represents 4 pixels, this value is set based on an internal column counter, which consists of two ranges, the default value corresponds to the first available pixel, <u>valid ranges:37–D5h - HS+1< HE</u>, See Figure 17. on page 23.</p>
18	Horizontal Window End	03	RW	<p>HE[7:0]- selects the ending point of HREF window.</p>
19	Vertical Window Start	05	RW	<p>VS[7:0] - selects the starting row of vertical window, <u>valid range: 05h ~ F5h. VS < VE</u> Interlace scan: each LSB represents 1 scan line in one field. Progressive scan: each LSB equals 2 scan line in one frame. In CIF (COMC5=1), it is 1 scan line. See Figure 17. on page 23.</p>
1A	Vertical Window End	F4	RW	<p>VE[7:0] - selects the ending row of vertical window.</p>
1B	Pixel Shift	34	RW	<p>PS[7:0] - to shift the output pixel timing relative to that of HREF, it physically shifts the video data output time early or late in unit of pixel clock as shown Figure 18. on page 23. This function is different from changing the size of the window as defined in registers HS & HE. The default corresponds to zero shift timing, lower value results in early pixel, higher value results in late pixel. If the amount of shift is beyond the physical image boundary, the black data will be used to filled the missing pixels. Lower than default number shifts the pixel in early(right) direction, since the lowest value is "00h", there are maximum 52 early pixels as 34h-00h = 52. Higher than default number shifts the pixel in delay(left) direction, the highest number is "FFh"; so maximum shift number is: Early: 52 pixels; Late: 204 pixels.</p>
1C	Manufacture ID (high)	7F	R	<p>MIDH[7:0] – Read only. Always returns '7F'.</p>
1D	Manufacture ID (low)	A2	R	<p>MIDL[7:0] – Read only. Always returns 'A2'.</p>
1E	Test A	C4	-	rsvd
1F	Test B	04	-	rsvd

Subaddress (hex)	Register	Default (hex)	Read/Write	Descriptions
20	Common E	00	RW	<p>COME7 - HREF pixel number selection. "1" - HREF include 720 PCLK and first 76 pixel data are black reference level, HE[7:0] and HS[7:0] should be kept at default value; "0" - HREF width decided by HS[7:0], HE[7:0] and COMA3=0.</p> <p>COME6 - Every line luminance average level and Field/Frame luminance, red, blue and green component average level output enable. "1" - Average level will be output from Y channel. "0" - disable average level output.</p> <p>COME5 - reserved</p> <p>COME4 - "1" aperture correction enable. Correction strength and threshold value will be decided by COMF[7:4]. "0" - Disable</p> <p>COME3 - S-AWB enable, effective only when COMB0=1 and COMA2=1</p> <p>COME2 - AWB method selection, effective only when COMB0=1 and COMA2=1. Enable condition is set by GAM[7:5].</p> <p>COME1 - AWB fast/slow mode selection. "1" - fast AWB, "0" - slow AWB. When AWB enable, COMA2=1, fast AWB (power up) then slow AWB.</p> <p>COME0 - Digital output driver capability. "1" High drivability for digital output. "0" low drivability.</p>
21	Y Offset	80	RW	<p>Y channel manual offset adjustment, effective when COMG[2]=1 YOF[7] - sign bit, "1" increase, "0" - decrease YOF[6:0] - Y channel offset</p>
22	UOffset	80	RW	<p>U channel manual offset adjustment, effective when COMG[2]=1 UOF[7] - sign bit, "1" increase, "0" - decrease UOF[6:0] - U channel offset value</p>
23	Rsvd23	40	-	rsvd
24	ECW	18(I)/2E(P)	RW	<p>Exposure white level setting for AEC. ** This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting. The following equation must be satisfied to ensure stable AEC. AEW<7:0> + AEB<7:0 > [4D] - Interlaced; AEW<7:0> + AEB<7:0 > [9A] - progressive</p>
25	ECB	3F(I)/7C(P)	RW	<p>Exposure black level setting for AEC. ** This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting. The following equation must be satisfied to ensure stable AEC. AEW<7:0> + AEB<7:0 > [4D] - Interlaced; AEW<7:0> + AEB<7:0 > [9A] - progressive</p>
26	Common F	80	RW	<p>COMF[7:6]: - digital aperture correction coring level [00] - 8 mV [01] - 16 mV [10] - 32 mV [11] - 64 mV.</p> <p>COMF[5:4]: digital aperture correction gain [00] - 0% [01] - 50% [10] - 100% [11] - 200%.</p> <p>COMF3 - reserved. COMF2 - swap MSB <-> LSB, default is bit7 = MSB. COMF1 - "1" enables A/D self-calibration. COMF0 - reserved.</p>
27	Common G	80	RW	<p>COMG[7:4] - rsvd, set to "C" for normal operation COMG[3] - rsvd, set to "0" for normal operation COMG[2] - "1" disable Y & U & V auto offset adjustment, Y or U or V offset can be manually set in Reg21 and Reg22 and Reg2E. COMG[1] - "1" disable CCIR601 range clip, data range extends to 01h - FEh. COMG[0] - rsvd</p>
28	Common H	00	RW	<p>COMH[7] - enable one-line output, valid in progressive scan COMH[6] - enable BW feature. COMH[5] - enable progressive scan COMH[4] - stop AEC/AGC, camera retains the last exposure/gain values. COMH[3] - stop AGC, camera retains the last gain value. COMH[2] - enable YG feature. COMH[1] - enable a fixed 2x gain in addition to the AGC control COMH[0] - higher AGC, "1" extends the AGC upper limit by 2x</p>
29	Common I	00	RW	<p>COMI[7] - stop AEC, camera retains the last exposure value. COMI[6] - enable external sync (slave) mode, hsync,vsync becomes input. COMI[5:4] - rsvd COMI[3] - "1" center exposure algorithm, "0" - area exposure algorithm COMI[2] - rsvd COMI[1:0] - version ID, read only</p>

Sub-address (hex)	Register	Default (hex)	Read/Write	Descriptions
2A	Frame Rate H	00	RW	EHS7 - Frame Rate adjustment enable bit. "1" Enable. EHS6:5 - Highest 2 bit of frame rate adjust control byte. see explanation below. EHS4 - "1" - UV component delay 2 pixel. "0" no 2*Tp delay. EHS3 - Y channel brightness adjustment enable. When COMF2=1 active. EHS2 - Always "1" EHS1 - Always "0" EHS0 - Always "0"
2B	Frame Rate L	00	RW	EHS7:0 - Lowest 8 bit of frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.12%. Range is 0.12% - 112%. IF frame rate adjustment enable, COME7 must set to "0".
2C	ALC	88	RW	EXBK[7:4] - Auto Level Control high level comparator selection. Range is 0.08% - 1.3% EXBK[3:0] - Auto Level Control step selection. Range is 0.08% - 1.3%.
2D	Common J	00	RW	COMJ7 - AEC update rate selection. "1" slow, "0" faster. COMJ6 - CIF 60 frame/s selection. "1" Only Odd field in Interlace Mode data output, "0" Odd/Even field data output, frame rate is 30 Frame/s. COMJ5 - ALC update rate selection. "1" slow, "0" fast. COMJ4 - Enable Auto Level Control. COMJ3 - reserved COMJ2 - Band filter enable. After adjust frame rate to match indoor light frequency, this bit enable a different exposure algorithm to remove light band seen under fluorescent light. COMJ1 - Always "1". COMJ0 - Always "1".
2E	VOffset	80	RW	V channel manual offset adjustment, effective when COMG[2]=1 VOF[7] - sign bit, "1" increase, "0" - decrease VOF[6:0] - V channel offset value
2F	Array Bias	50	RW	Array bias adjustment, use factory setting only
30	Red Matrix	31	RW	RMX[7:0] - rgb matrix red coeff
31	Green Matrix	61	RW	GMX[7:0] - rgb matrix green coeff
32	Blue Matrix	DC	RW	BMX[7:0] -rgb matrix blue coeff
33	Rsvd33	80	RW	rsvd
34	Bias Adjust	69	RW	BAJ[7:6] : A/D reference level adjustment. [00] - 110% internal full signal range; [01] - 120%, [10] - 130%, [11] - 140%. BAJ[5:4]: UV low-pass-filter bandwidth selection. [00] - 0.4MHz, [01] - 0.8 MHz, [10] - 1.2MHz, [11] - 1.6 MHz. BAJ[3:2]: signal peak level adjustment. [00] - 70% of full range, [01] - 80%, [10] - 90%, [11] - 100% of full range. BAJ[1:0]: clip voltage selection. [00] - 2.4v, [01] - 2.6v, [10] - 2.8v, [11] - 3.0V
35	Common L	54	RW	COML[7:5] - Y channel delay time selection relative to UV channel COML[4] - enable UV Filter 1 COML[3] - enable UV Filter 2 COML[2] - Y signal algorithm selections. COML[1] - Always "1". COML[0] - reserved.
36	Rsvd36		RW	rsvd
37	Rsvd37		RW	rsvd
38	Common K	81	RW	COMK7 - HREF edge selection w.r.t PCLK "1" - PCLK falling edge "0" - PCLK rising edge. COMK6 - High driveability for digital output pin. COMK5 - reserved. COMK4 - ZV port Vertical timing selection. "1" VSYNC output ZV port vertical sync signal. "0" normal TV vertical sync signal. COMK3 - Quick stable mode when camera mode change. (CIF, 8 Bit output, CCIR 656 mode and Progressive Scan Mode). After relative control bit set, the first VS will be the stable image with suitable AEC/AWB setting. "0" - slow mode, after mode change need more field/frame to get stable AEC/AWB setting image. COMK2 - reserved. COMK1 - AWB settle time selection for slow AWB operation. "1" - fast "0" - slow. COMK0 - Always "1"

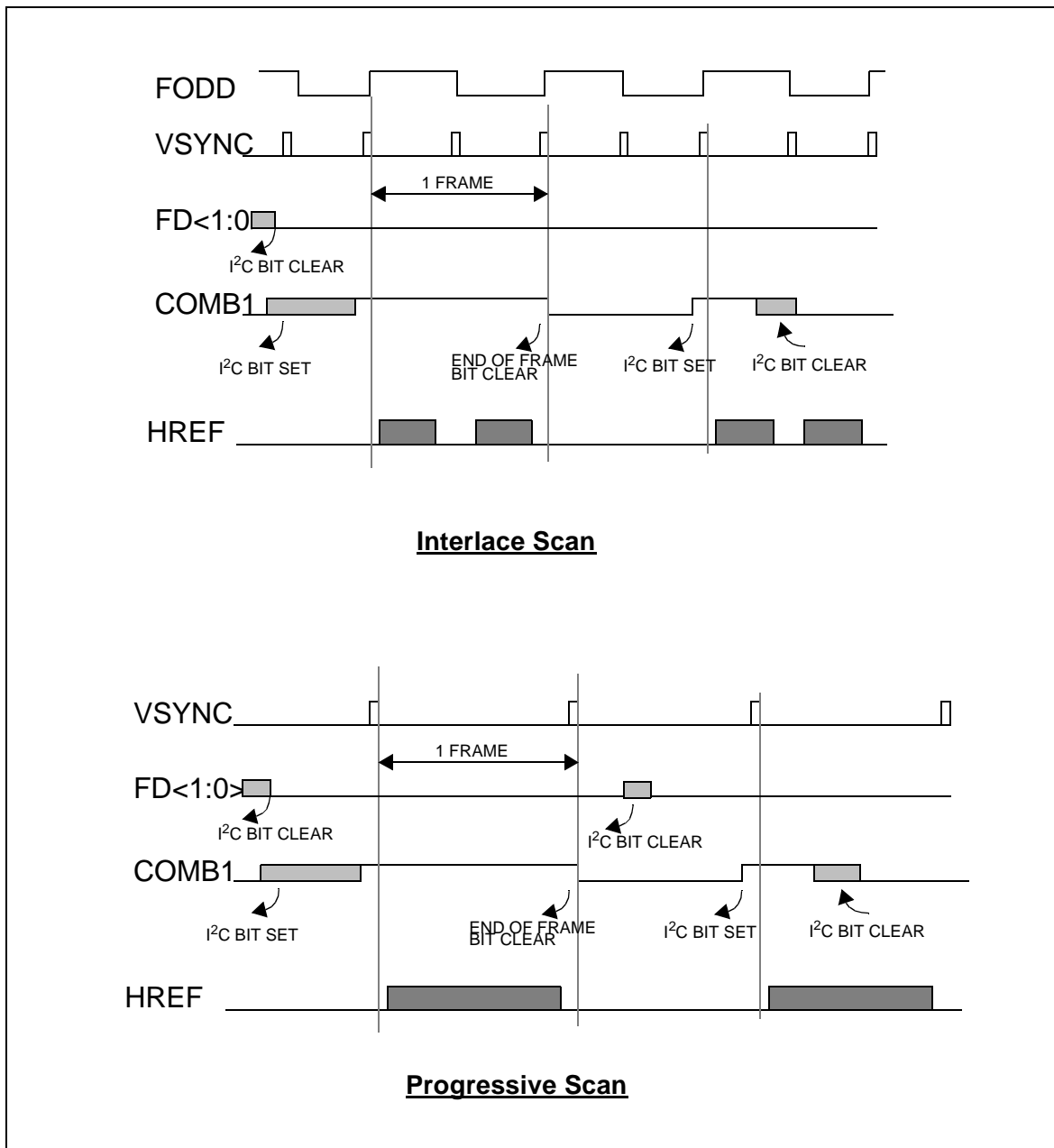


Figure 15. Single Frame Transfer Example

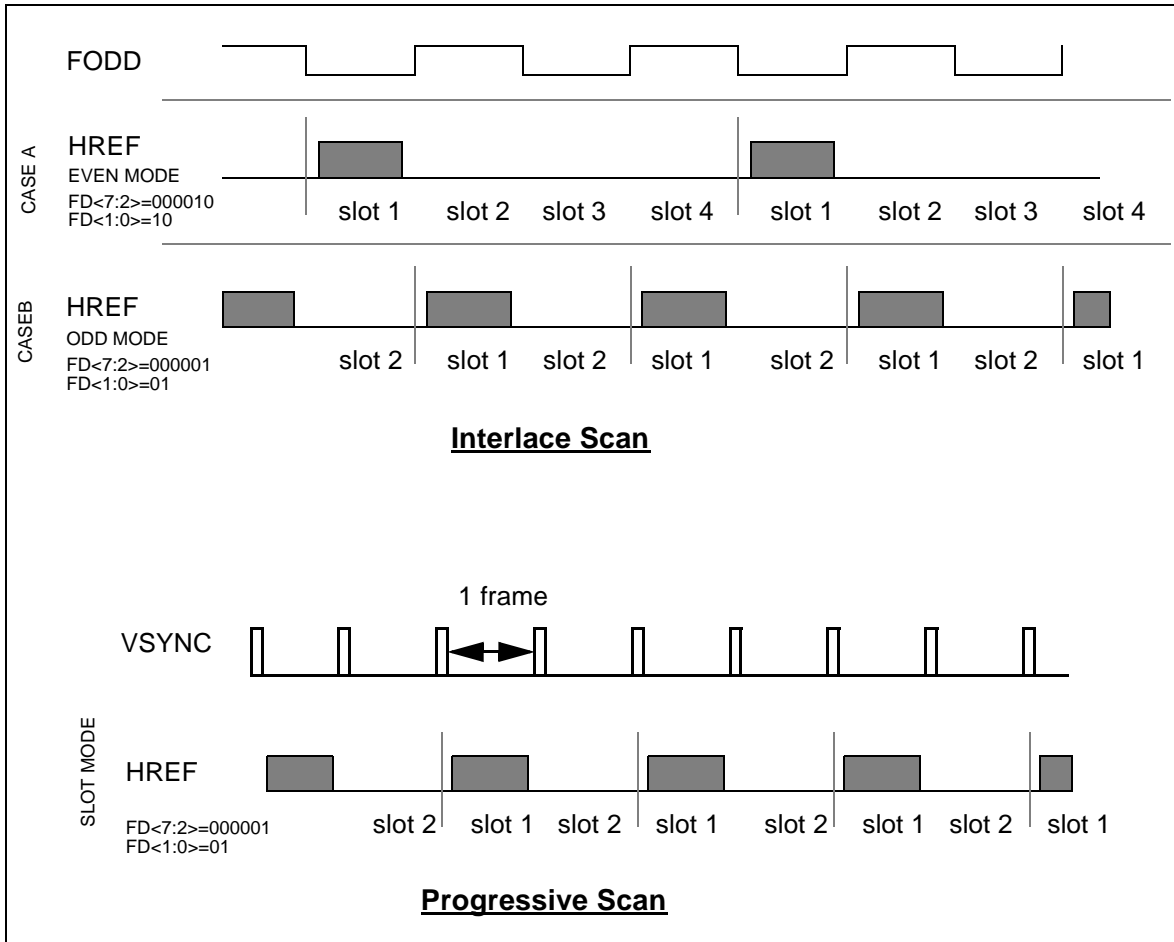


Figure 16. Field Division Example

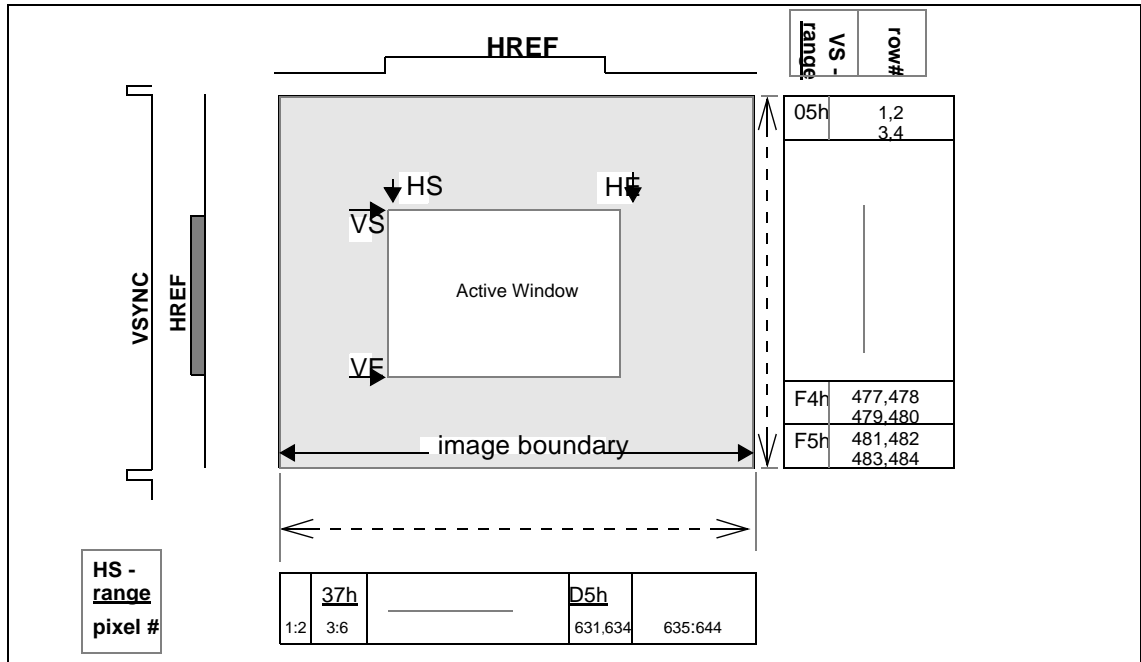


Figure 17. Window Sizing

Note 1. Valid End value must be "higher than" Start value for both VE/VS and HE/HS. At minimum, (VE-VS)=1 equals 4 rows, (HE-HS)=1 equals 4 pixels. Horizontal counter has two region, the counter wraps back to 00h after reaching D6h.

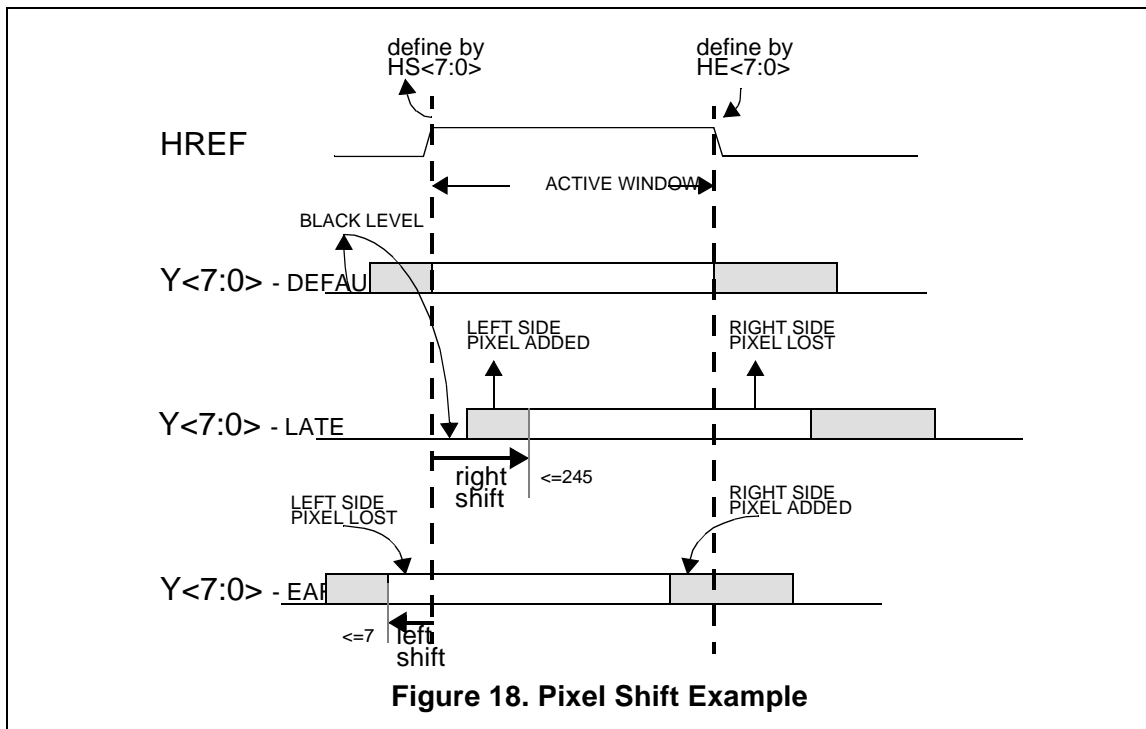


Figure 18. Pixel Shift Example

Note: pixel shift feature does not affect the order of video data in Y and UV bus.

8. Specifications**Table 4. Electrical parameters** (0°C to 70 °C, all voltages referenced to GND)

Symbol	Descriptions	Max	Type	Min	Units
Supply					
V _{DD}	Supply voltage (VDD, DVDD)	5.5	5.0	4.5	V
V _{DDO}	Supply voltage (DOVDD)	3	-	5.5	V
I _{DD1}	Supply Current in VDDs	25	-	-	mA
I _{DD2}	Supply Current in DOVDD @ 50pf load at digital output	-	40	-	mA
I _{DD3}	Standby supply current (CMOS level @ inputs)	100	-	-	uA
Digital input pin					
V _{IL}	Input voltage LOW	0.8	-	-	V
V _{IH}	Input voltage HIGH	-	-	2.0	V
C _{in}	Input capacitor	10	-	-	pF
t _r , t _f	Digital input rise/fall time	25	-	-	ns
Digital output - standard load 50pf, 1.2kΩ to 3.0volts					
V _{OH}	Output voltage HIGH	-	-	2.4	V
V _{OL}	Output voltage LOW	0.6	-	-	V
Video bus - (@ 60Hz fps)					
t _{PCLK}	PCLK cycle time	-	74	-	ns
t _p	PCLK pulse width	-	32	-	ns
t _{DS}	data to PCLK set up time	-	t _p - 10	-	ns
t _{DH}	data to PCLK hold time	-	t _p - 10	-	ns
I²C					
f _{scl}	SCL clock frequency	400	-	-	kHz
t _f	SDA fall time	300	-	20 + 0.1C _{sda}	ns
t _{idle}	Bus idle time	-	-	1.3	us
t _{hdsta}	START hole time	-	-	0.6	us
t _{stps}	STOP set up time	-	-	0.6	us
t _{ds}	SDA set up time	-	-	100	us
t _{dh}	SDA hold time	-	-	0	us
Clock input / Crystal Oscillator					
f _{osc}	Resonator frequency	3	27.000	30	MHz
	Load capacitor	-	10	-	pF
	Parallel resistance	-	1M	-	W
	Rise/fall time for external clock input	-	5	-	ns
	Duty cycle for external clock input	60	-	40	%
Misc. timing					
t _{SYNC}	External FSI cycle time	-	2	-	frame
t _{PU}	Chip power up time	100	-	-	us
t _{PD}	Power up delay time	-	10	-	us
t _{PZ}	Power up low-z delay	-	1000	-	ns
VTO analog video output parameters					
V _{TO-P}	video peak signal level	-	1.9	-	V

Table 4. Electrical parameters (0°C to 70 °C, all voltages referenced to GND) (Continued)

Symbol	Descriptions	Max	Type	Min	Units
V _{TO-B}	video black signal level	-	1.0	-	V
V _{SYNC}	Y video sync pulse amplitude	-	0.6	-	V
R _o	Video output load	-	75	-	Ohm
t _H	horizontal line width				pclk
t _{HSYNC}	horizontal sync width		858		pclk
t _{HBK}	horizontal blank width		64		pclk
t _V	vertical field width		262.5		t _H
t _{VSYNC}	vertical sync width		3		t _H
t _{VF1}	field 1 vertical front equalization width		3		t _H
t _{VB1}	field 1 vertical back equalization width		3		t _H
t _{VBK1}	field 1 blank line outside equalization region		11		t _H
t _{VF2}	field 2 vertical front equalization width		3.5		t _H
t _{VB2}	field 2 vertical back equalization width		3		t _H
t _{VBK2}	field 2 blank line outside equalization region		11.5		t _H

Table 5. Sensor Characteristics (temperature 27 °C, illumination 3200 °K, pixel leakage doubles every 10 °C)

Parameter	Value	Units	Descriptions
Sensitive	20 (color) 2 (BW)	lux	AGC 4x, $\gamma=1$, lens f1.4, CM500 t=1mm IR (color) measured rms value at 50 IRE signal level
Dynamic Range	72	dB	AGC off, $\gamma=1$, AEC on
Random Noise	-38(color) -40(BW)	dB	AGC 4x, $\gamma=1$ measured rms value at 75% signal illumination level vs full scale
Fix pattern Noise	-42(color) -42(BW)	dB	AGC 4x, $\gamma=1$ measured rms value at 75% signal illumination level vs full scale
Smear	<0.03	%	
Blooming	<0.01	%	

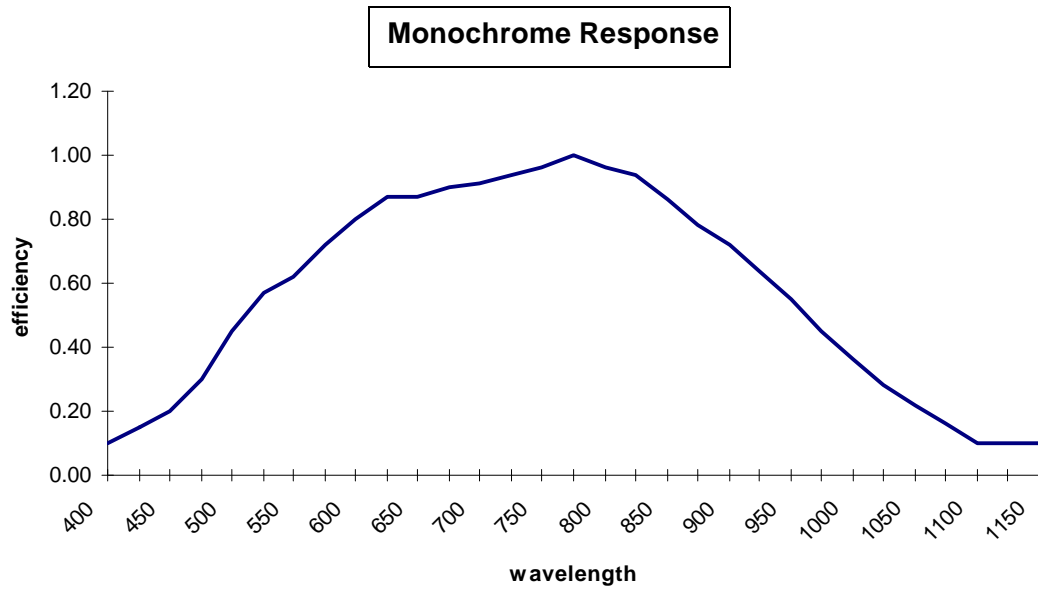
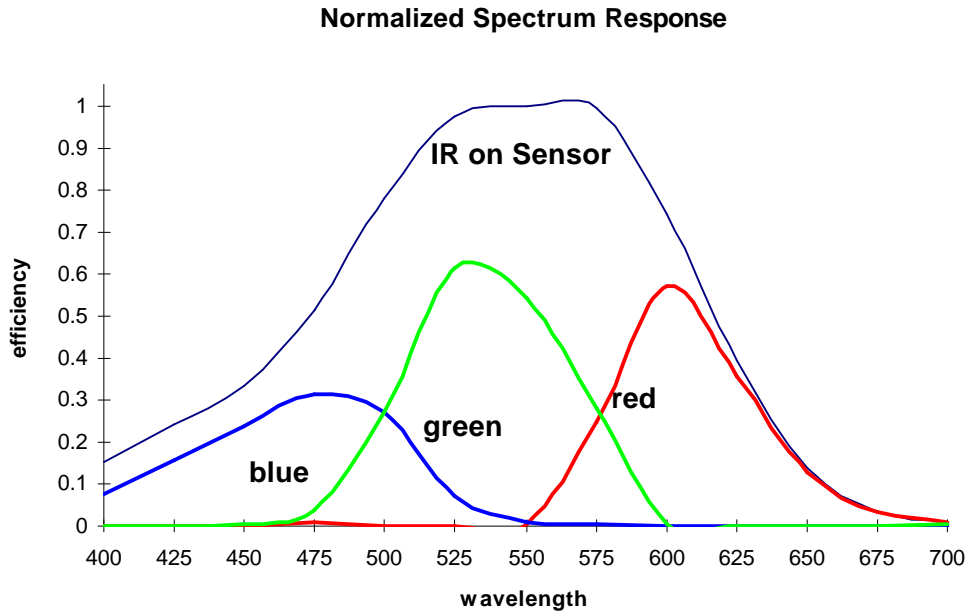


Figure 19. Spectrum Response

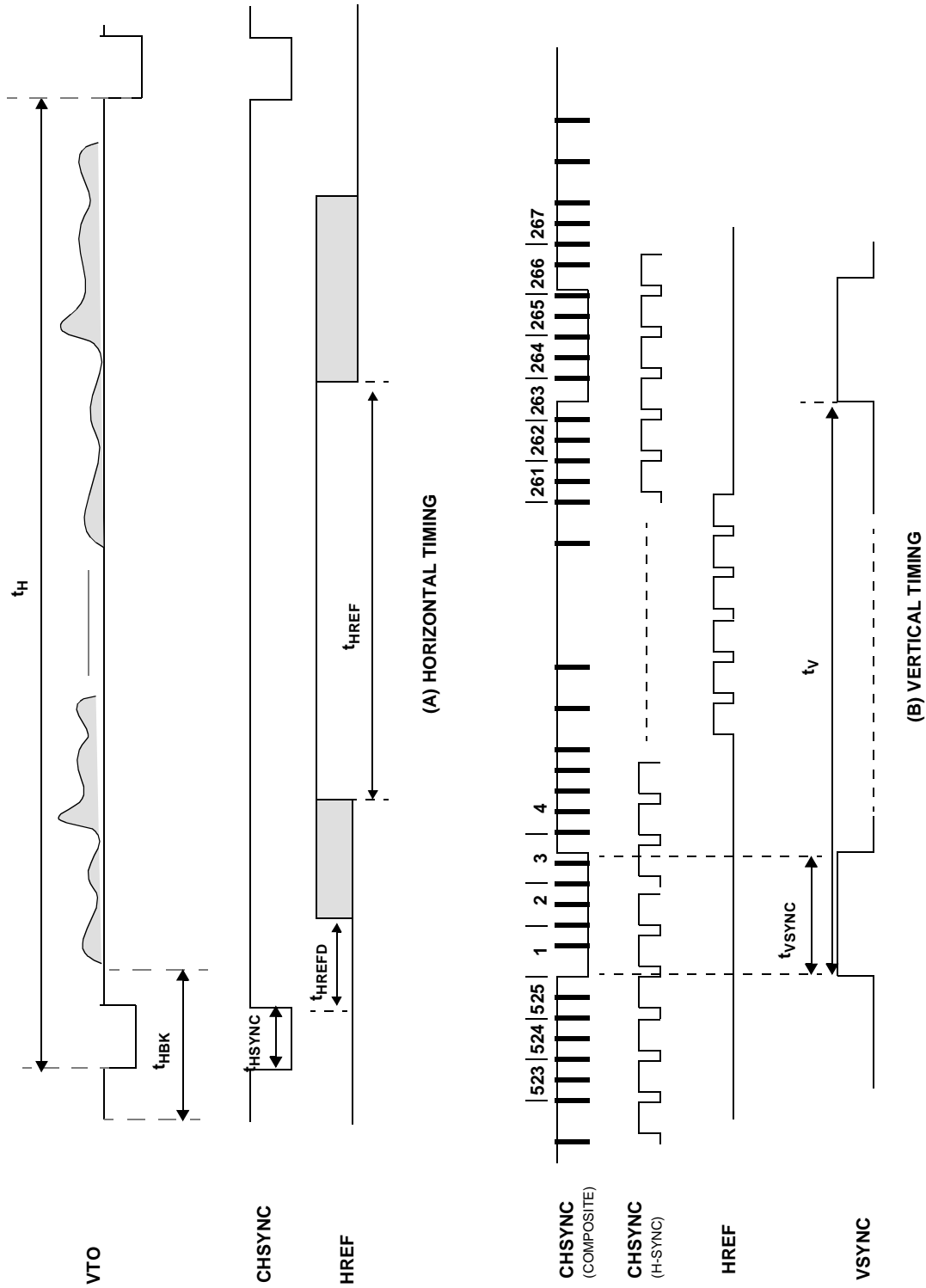


Figure 20. Video Timing Diagram

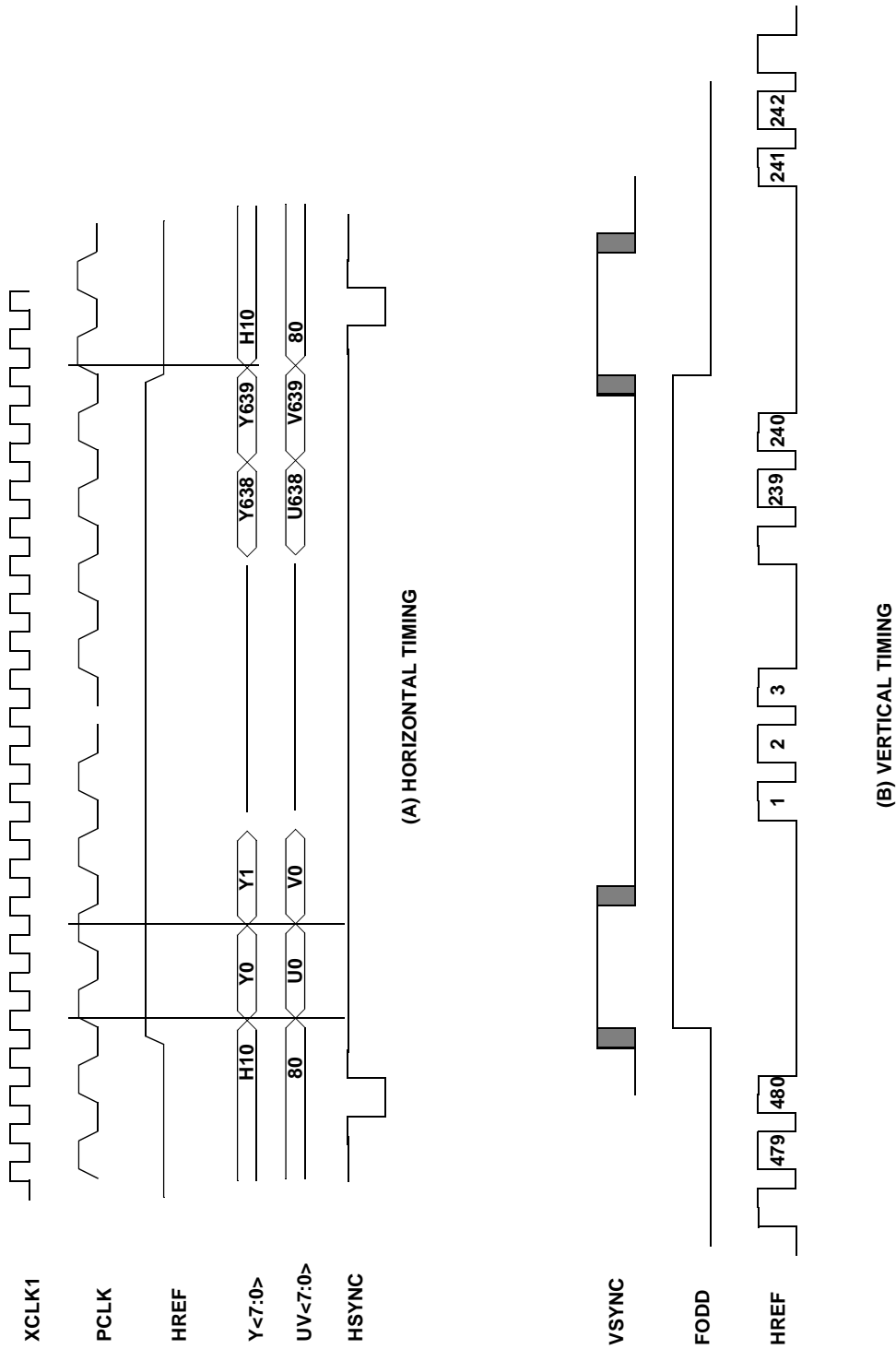


Figure 21. Digital Data Bus Timing

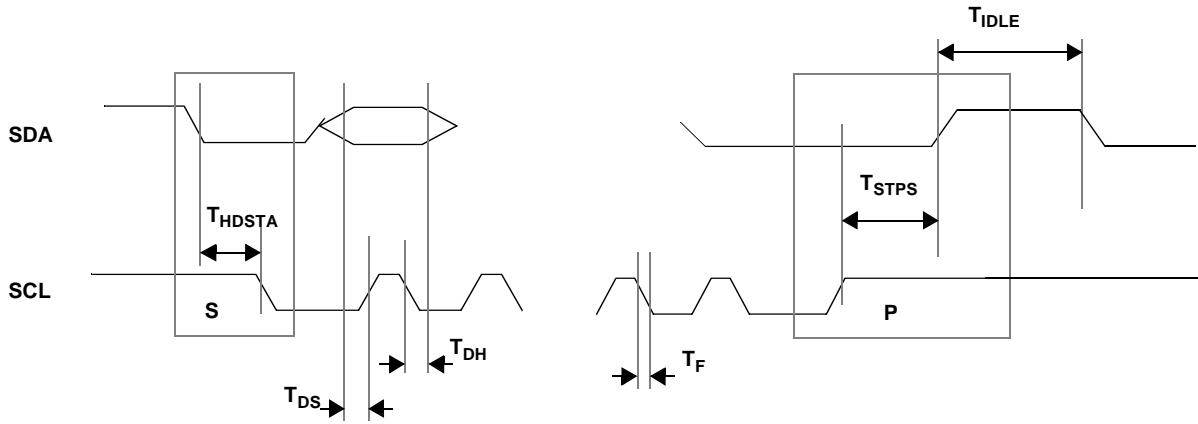


Figure 22. I²C Bus Timing

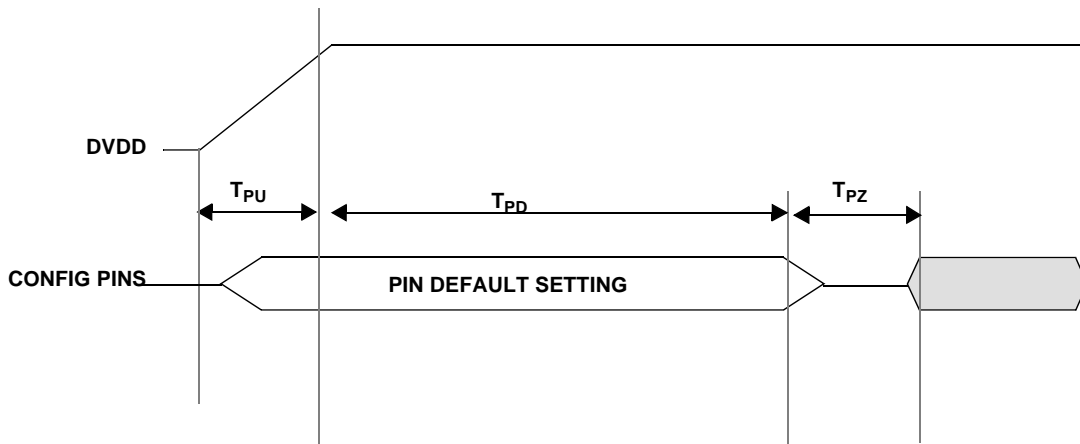


Figure 23. Configuration Pin Setting at Power Up

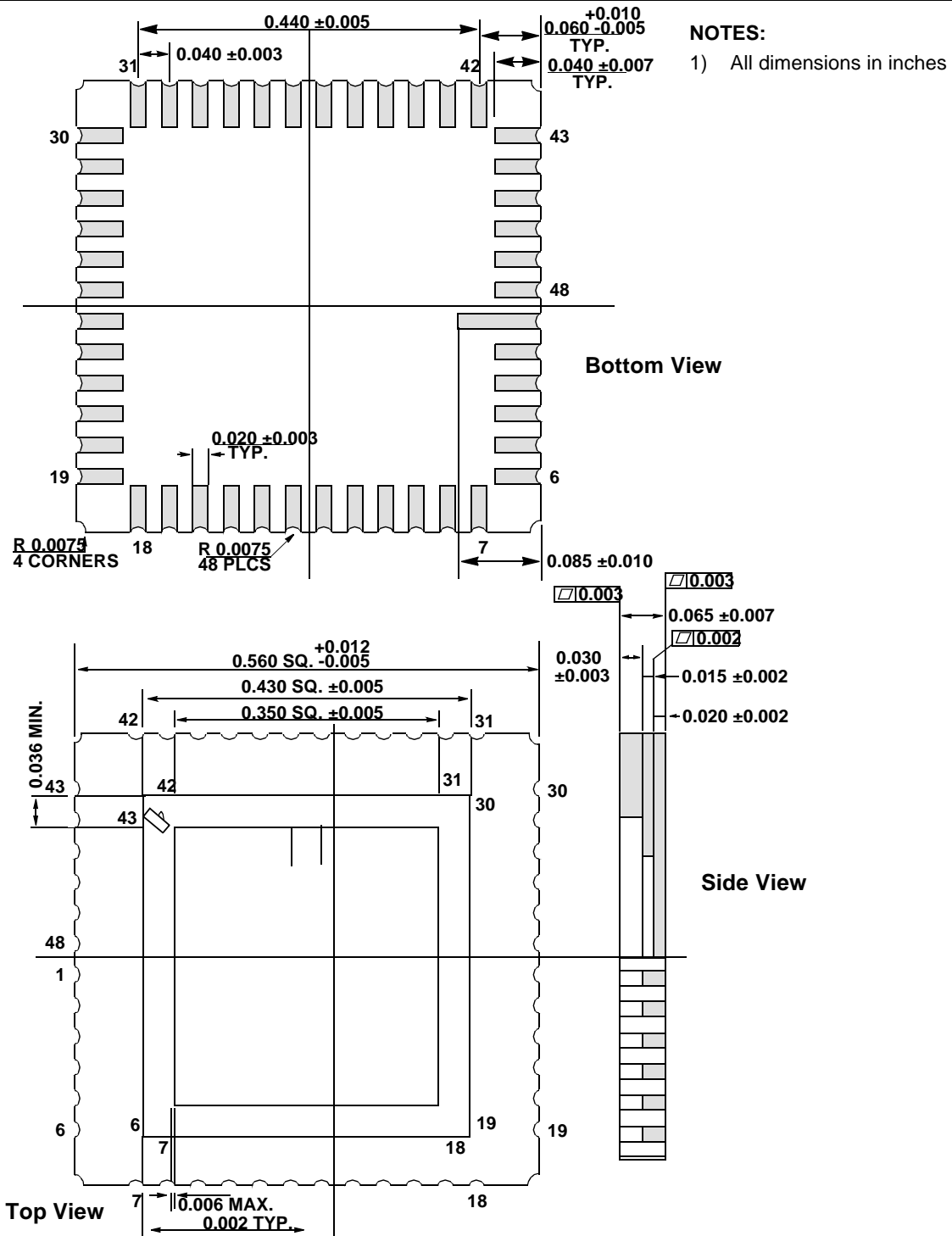


Figure 24. Package Mechanical Data

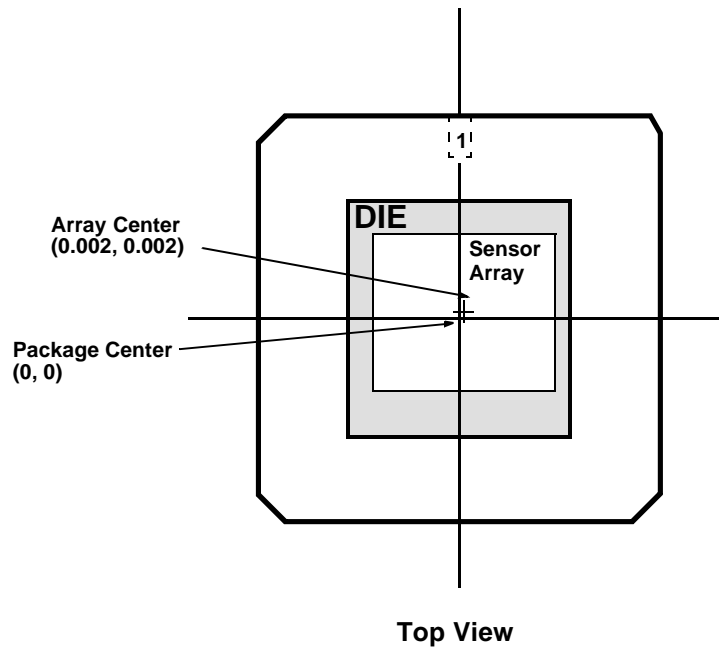


Figure 25. OV7610 Sensor Array Location (in inches)

Ordering Information

Part Number	Description	Comments
OV7610	Color Digital Sensor	48 pin LCC
OV7110	Monochrome Digital Sensor	48 pin LCC
OV7610A	Color Digital camera evaluation board	Contact Factory

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Appendix

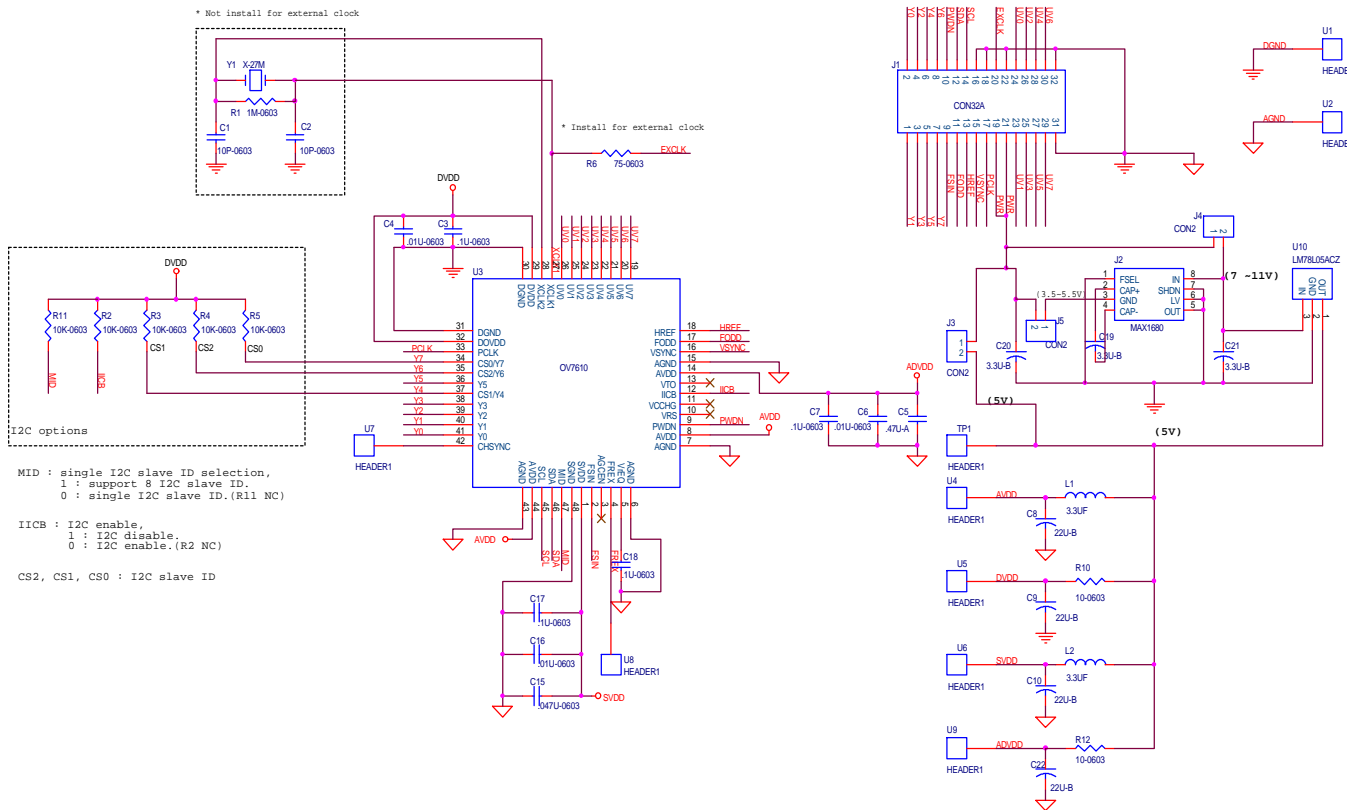
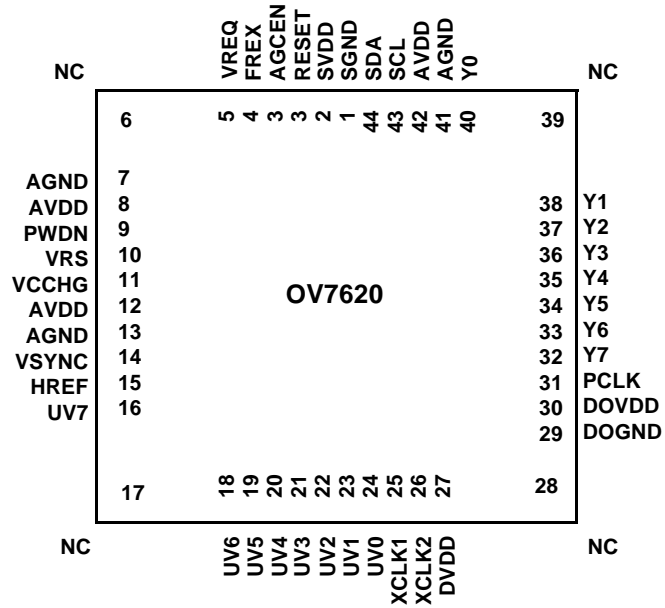


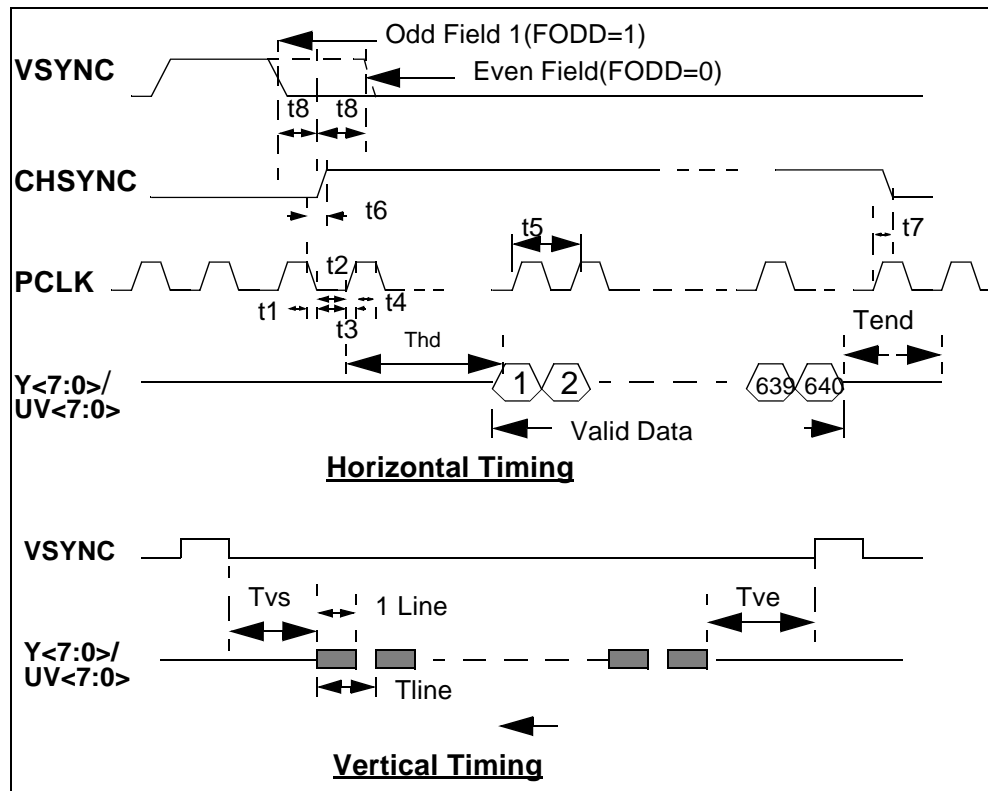
Figure 26. Referencing digital camera design



44pin package pin out diagram

ZV PORT Timing:

The ZV Port is a single-source unidirectional video bus between a PC Card socket and a VGA controller. The ZV Port complies with CCIR601 timing to allow NTSC decoders to deliver real-time digital video straight into the VGA frame buffer from a PC Card. OV7600 support ZV Port Timing, which output signal can be output to a PC Card directly, then to VGA controller. ZV Port Timing



Notes: ZV Port format output signal include

- VSYNC:** Vertical sync pulse.
- CHSYNC:** Horizontal sync pulse.
- PCLK:** Pixel clock used to clock valid data and CHSYNC into ZV Port. Default frequency is 13.5MHz when use 27MHz as system clock. Rising edge of PCLK is used to clock the 16 Bit data.
- Y<7:0>:** 8 Bit luminance data bus.
- UV<7:0>:** 8 Bit chrominance data bus.
- Note: In Interlaced Mode, there are Even/Odd field different (t8). When In Progressive Scan Mode, only frame timing same as Even field(t8).

Table A1: ZV Port AC Parameter

Symbol	Parameter	Min.	Max.
t1	PCLK fall timing	4 ns	8 ns
t2	PCLK low time	30 ns	
t3	PCLK rise time	4 ns	8 ns
t4	PCLK high time	30 ns	
t5	PCLK period	74 ns	
t6	Y/UV/CHSYNC setup time	10 ns	
t7	Y/UV/CHSYNC hold time	20 ns	
t8	VSYNC setup/hold time to CHSYNC	1 us	

Thd is the pixel number between 1st valid data and 1st PCLK rising after CHSYNC rising edge. When in default horizontal window setting, **Thd** = 142*t5, which is changed with register HS<7:0>. HS<7:0> increase 1, **Thd** increase 4 pixel clock.

Tend is the pixel number between last valid data and 1st PCLK rising edge after CHSYNC falling edge. When in default horizontal window setting, **Tend** = 10*t5, which is changed with register HE<7:0>. HE<7:0> change 1, **Tend** change 4 pixel clock.

After VSYNC falling edge, OV7600 will output black reference level, the line number is **Tvs**, which is the line number between the 1st CHSYNC rising edge after VSYNC falling edge and 1st valid data CHSYNC rising edge. Then valid data, then black reference, line number is **Tve**, which is the line number between last valid data CHSYNC rising edge and 1st CHSYNC rising edge after VSYNC rising edge. The black reference output line number is dependent on vertical window setting.

When in default setting, **Tvs** = 14*Tline, which is changed with register VS<7:0>. If in **Interlaced Mode**, VS<7:0> change 1 step, **Tvs** increase 1 line. If in **Progressive Scan Mode**, VS<7:0> step equal to 2 line.

When in default setting, **Tve** = 4*Tline for **Odd Field**, **Tve** = 3*Tline for **Even Field**, which is changed with register VE<7:0>. If in **Interlaced Mode**, VE<7:0> change 1 step, **Tve** increase 1 line. If in **Progressive Scan Mode**, VE<7:0> step equal to 2 line.

In **Progressive Scan Mode**, **Tve** = 3*Tline and **Tvs** = 35*Tline.